CURSO DE ELECTRONICA IV
Alfonso Pérez García.

INDICE.

1 PROGRAMA.

SEP. DIRECCIÓN GENERAL DE INSTITUTOS TECNOLÓGICOS SEIT.
1. IDENTIFICACION DEL PROGRAMA DESARROLLADO POR UNIDADES DE APRENDIZAJE.

NOMBRE DE LA ASIGNATURA:	**ELECTRONICAIV (4-2-10).**
NIVEL:	**LICENCIATURA.**
CARRERA:	**INGENIERIA ELECTRONICA.**
CLAVE:	**ECC 9327**

NUMERO	TEMA	SUBTEMAS:		DURACION	EVAL.
I	**Circuitos Integrados especiales.**	**1.1** Osciladores controlados por voltaje.(VCO) **1.2** Circuitos de Amarre de fase.(PLL)	**1.3** Modulador de ancho de pulso. **1.4** Estructura y ecuaciones de diseño.	**3 SEMANAS** **12 HORAS**	**50% EE** **50% EP**
II	**Fuentes de alimentación conmutadas.**	**2.1** Conceptos básicos **2.2** Configuraciones básicas CD-CD y fijas. **2.3** Etapas entrada-salida. **2.4** Circuiteria de control.	**2.5** Circuiteria de protección y auxiliar. **2.6** Estándares de seguridad eléctrica.	**3 SEMANAS** **12 HORAS**	**100% EP**
III	**Acondicionamiento de señales.**	**3.1** Linealización. **3.2** Filtrado.	**3.3** Escalamiento; tiempo, **3.4** Multiplicación..	**2 SEMANAS** **8 HORAS**	**50% EE** **50% EP**
IV	**Aplicaciones y proyecto.**	**4.1** . **4.2** .	**4.3** .	**7 SEMANAS** **28 HORAS**	**100% EP**

BIBLIOGRAFIA.

AUTOR	TITULO	EDITORIAL
	WWW.HOWSTUFFWORKS.COM	**www.analog.com**
	WWW.NSC.COM	**www.ni.com**
	POWER INTEGRATION SITE	**www.maxim-ic.com**
	TEXAS INSTRUMENTS SITE	
	LITEON SITE	
	MOTOROLA SITE (freescale)	

2 UNIDAD 1. Circuitos Integrado Especiales.

2.1 Introducción y Conceptos básicos.

2.1.1 "Amplifiers oscillate and oscillators amplify" - unknown

2.1.1.1 Introduction

When I was a kid, yes I can remember back to the late 1940's, we collected all manner of junk. Cool was anything remotely electrical and, of course bicycle dynamos, lamps or motors were even "extra cool".
We as precious little seven year olds conceived - all budding nuclear physicists that we were - of this real smart idea, obviously nobody had ever thought of this before.

"Why don't we connect a motor to a generator, so
the motor drives the generator, providing electricity
for the motor, which continues to drive the
generator and it'll go on, and on, and on for a
hundred years and we'll become world famous!"

Of course we had no concept of frictional losses (I think that's right) way back then. Nor had the words "perpetual motion" passed our ears.
The whole point of that little story is to crudely demonstrate the principle of how an oscillator works. If you can follow that childishly naive concept then you will kill them in this.

2.1.1.2 Principles of Oscillator operation

Every oscillator has at least one active device (smarties don't complicate matters for me - just read on) be it a transistor or even the old valve. This active device and, for this tutorial we'll stick to the humble transistor, acts as an amplifier. There is nothing flash about that. For this first part of the discussion we will confine ourselves to LC Oscillators and I'll keep the maths to an absolute minimum.
At turn on, when power is first applied, random noise is generated within our active device and then amplified. This noise is fed back positively through frequency selective circuits to the input where it is amplified again and so on, a bit like my childhood project. Ultimately a state of equilibrium is reached where the losses in the circuit are made good by consuming power from the power supply and the frequency of oscillation is determined by the external components, be they inductors and capacitors (L.C.) or a crystal. The amount of positive feedback to sustain oscillation is also determined by external components.

2.1.1.3 Hartley Oscillator

I decided to lead off with this one for the simple reason it's my favourite. Recently it was discussed that your favourite oscillator was likely the one which worked best for you and I think that is quite true. So here it is in it's most simplified form.

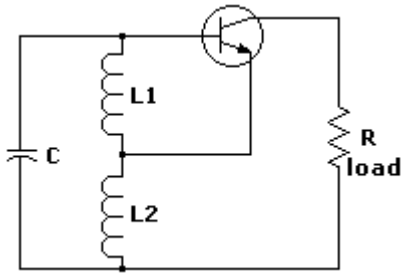


Fig 1.

2.1.1.4 Colpitts Oscillator

The basic Colpitts oscillator circuit look like this and you will see some similarities.

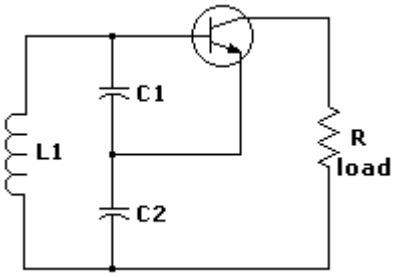


Fig 2.

If you consider positive feedback is applied to compensate for the losses in the tuned circuit, the amplifier and feedback circuit create a negative resistor. When Z1 and Z2 are capacitive, the impedance across the capacitors can be estimated from a formula I won't lay on you here because it includes beta, hie, as well as X_{C1} and X_{C2}. Suffice to say it can be shown that the input impedance is a negative resistor in series with C1 and C2. And the frequency is in accordance with:

$$fo = \frac{1}{2\pi [LC_1C_2/(C_1+C_2)]^{1/2}}$$

Fig 3.

2.1.1.5 Frequency or Phase Stability

Frequency or phase stability of an oscillator is customarily considered in the long term stability case where frequency changes are measured over minutes, hours, days even years. Of interest here are the effects of the components changes, with ambient conditions, on the frequency of oscillation. These might be caused by changes in the input voltage, variations in temperature, humidity and ageing of our components.

Never underestimate the effects of these variations on the frequency of operation. I've gone nuts working on so called precision designs, with precision components, where the frequency wandered at random over several kilohertz over several minutes. Needless to say I'd "messed up".
Short term stability is also of great interest and, again I could lay some real heavy maths on you but I won't. I'll simply say it can be mathematically proven that the higher the circuit Q, the higher this stability factor becomes. The higher the circuit Q, the better the ability the tuned circuit can filter out undesired harmonics **AND** noise.

2.1.1.6 Reducing Phase Noise

- 1. Maximize the Qu of the resonator.
- 2. Maximize reactive energy by means of a high RF voltage across the resonator. Use a low LC ratio.
- 3. Avoid device saturation and try to use anti parallel (back to back) tuning diodes.
- 4. Choose your active device with the lowest NF.
- 5. Choose a device with low flicker noise, this can be reduced by RF feedback. A bipolar transistor with an unby-passed emitter resistor of 10 to 30 ohms can improve flicker noise by as much as 40 dB.
- 6. The output circuits should be isolated from the oscillator circuit and take as little power as possible.

2.1.1.7 Effects of ambient changes on stability

A frequency change of a few tens of hertz back and forth over a couple of minutes would mean nothing to an entertainment receiver designed for the FM Radio band. Such a drift in an otherwise contest grade receiver designed to receive CW (morse code) would be intolerable. It's a question of relativity.

2.1.1.8 Minimizing Frequency drift

These are random and not in any particular order.

- 1. Isolate the oscillator from succeeding stages with a well designed buffer stage followed by a stage of amplification. Large signals can often then be reduced by a 3 or 6 dB attenuator which also has the benefit of presenting a well defined load impedance to the amplifier. If the stage is feeding a mixer, as is most often the case, then another benefit is the mixer (you are using double balanced mixers?), also see a source impedance of 50 ohms.

- 2. Ensure the mechanical stability of your oscillator is such that mechanical vibration can have no effect on components, especially those frequency determining components.

- 3. Supply the oscillator with a clean well regulated supply. If using varactor tuning, doubly ensure the tuning DC voltage is as clean as possible, a few hundred micro volts of noise can be imposed on the oscillator signal. Use back to back diodes for the variable element. Air variables are hard to come by although they offer far superior Q figures. DC tuning tends to be more versatile.

- 4. Minimize circuit changes from ambient variations by using NPO capacitors, polystyrene are dearer but excellent, silvered mica in my opinion are not what many people believe and are highly over rated.

- 5. The inductor should be air wound on a coil form with a configuration to maximize Qu. If you must use a toroid, where possible try to use the 6 type as it offers the best Q. Sometimes, for other reasons you might have to use a slug tuned form.

- 6. Parallel a number of smaller value NPO capacitors rather than using one large one in frequency determining components. For trimmers try and use an air variable. Keep an eye out for small value N750, N1500 capacitors, < 15 pF, when available and are found to be dirt cheap. These are sometimes useful in taming drift in an oscillator.

- 7. Bipolar or FETS for active device seems to be a matter of personal preference and I've seen some ferocious arguments over that one. Consensus seems to come down in favour of FETS. Me, I'm a bipolar man because FETS hate me pure and simple.

So there are some of the things to keep in mind. Hopefully at this point you have discovered the broad idea of an oscillator, I've outlined broadly two types Hartley and Colpitts. I spoken about frequency stability and listed ways to combat phase noise and reducing frequency drift. Now let's proceed to the main course.

2.1.1.9 Designing a Hartley Oscillator

Here I'll present the schematic for my old favourite, together with a buffer stage and an amplifier stage which should deliver about 5V P/P into a 50 ohm load. We'll discuss each relevant stage and produce some rule-of-thumb design info. Because the consensus comes down in favour of FETS and I'm big enough to lay aside my prejudices in the noble cause of

advanced education we'll use a FET oscillator. Nothing to do with a few friends who might belt me up!

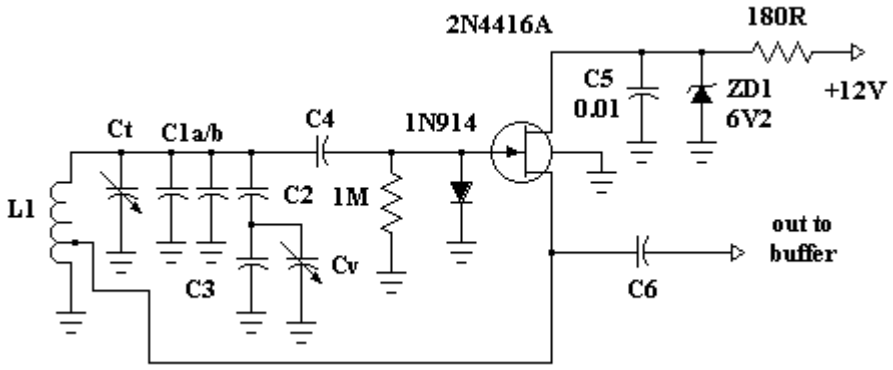


Fig 4.

For this design I'm going to say we will be constructing a general purpose VFO to operate at 5000 - 5100 Khz no particular reason, pick anything you like.

Now I chose a 2N4416A FET purely because I bought a big bag of them years ago and have them on hand. You could use any general purpose JFET you can readily obtain. Note the 2N4416A is a metal can and the case is grounded.

The frequency determining components are L1, Ct (a nominal 10 pf trimmer), C1a, C1b, C2, C3, Cv and C4.

Note: I have been asked a number of times the function of C4 in this circuit. Capacitor C4 is to reduce the loading on the tuned circuit components. It may be as small as possible consistent with being able to provide sufficient drive to the succeeding buffer amplifier stage. Often the home constructor will often make C4 a trimmer.

The other components are bog standard. The two resistors, silicon diode and zener diode need never change, capacitor C5 is about right for this frequency. C6 can be selected to give higher / lower output to the buffer amplifier. Smaller C6 values give lower output and conversely higher values give larger output.

The silicon diode I'll explain later, the zener diode is to give a regulated 6.2 volt supply

Now there is NOTHING sacred about my frequency determining capacitor combination O.K.? Too many people look at these kind of circuits and think they must duplicate everything literally, not so. This is just a typical representation. C1 to C3 plus Cv and Ct are just a combination of parallel and some series capacitors all designed to give us a bit of flexibility with the tuning range. Cv could easily be replaced by two back to back tuning diodes.

What you need to do to get the circuit to work is to have an inductive reactance for L1 of around about 180 ohms. At 5 Mhz this works out at about 5.7 uH and, if you don't know how I arrived at that figure I seriously recommend you spend some time on my other tutorials on my new site such as Basics and LC Filters.

The important aspect is that the feedback point from the source of the JFET connects to about 25% of the windings of L1 from the ground end. Now I've depicted an air cored inductor. It could be, just as one example among a great many, 18 - 19 turns of #20 gauge wire on a 25.4 mm (1") diameter form spread evenly over a length of about 25.4 mm (1").

The tap would be at about 4 1/2 turns. Check that out with the formula's I taught you elsewhere.
Alternatively, with degraded performance, you could use a T50-6 toroid and wind say 37 turns of #24 wire (5.48 uH) tapping at 9 turns. The A_L factor for a T50-6 is 40. Again do the other tutorials if necessary, I'm not going to repeat old work and it's going to be even harder from here on. I'll thoroughly explain new concepts, not the old.
So if we are to have our oscillator working at about 5 Mhz, we know the LC is 1013 and if L is say 5.7 uH then total C for resonance (just like LC Filters eh!) is about 177 pF. We want to be able to tune from 5000 to 5100 Khz a tuning ratio of 1.02 which means a capacitance ratio of 1.04 (min to max.).
Let's fiddle with some numbers! I have a Jackson Bros. air variable capacitor (very Rolls-Royce) which swings from 10.5 pF to 105 pF, a typical 10:1 ratio in air variables. This I will use for Cv.
If the total swing is 1.04 (actually 1.0404:1) and Cmax is 177 pF it follows Cmin is 170 pF. A variation of only 7 pF (roughly). Now we're treading on unsafe ground here with such a large variable capacitor. We could:

A)rip plates of it to reduce capacitance (don't even think about it)
B) go to varactor diodes with a small swing. That's O.K. but performance becomes degraded.
C) obtain a smaller air variable with Cmax of say 25 pF.

Just to prove I'm a glutton for punishment and if you're still here so are you, we will purely for the mathematical exercise, persevere with the 105 pF variable. What if we eliminate C3 and make C2 = 15 pF NPO then the series combination of C2 and Cv swing 6.176 pF to 13.125 pF, a variation of over 6.9 pF - are you lost? Go back to the other tutorials.
If our Cmax was 177 pF then 177 - 13.125 = 163.875 and the 177 pF was approximate anyway. I'd make Ct a 10 pF air trimmer (if available, if not, a ceramic or whatever the supplier offers but 10 pF max.). That leaves about 154 pF to make up. How about making C1a and C1b into 3 NPO capacitors of say 2 X 47 pF and 1 X 56 pF all NPO types. In total that comes to less than 177 pF max. but don't forget there are stray capacitance's in the circuit. In the final wash-up you could simply use 3 X 47 pF.
Next voltage controlled oscillators.

2.1.2 Introduction to Fundamental Crystal Oscillators

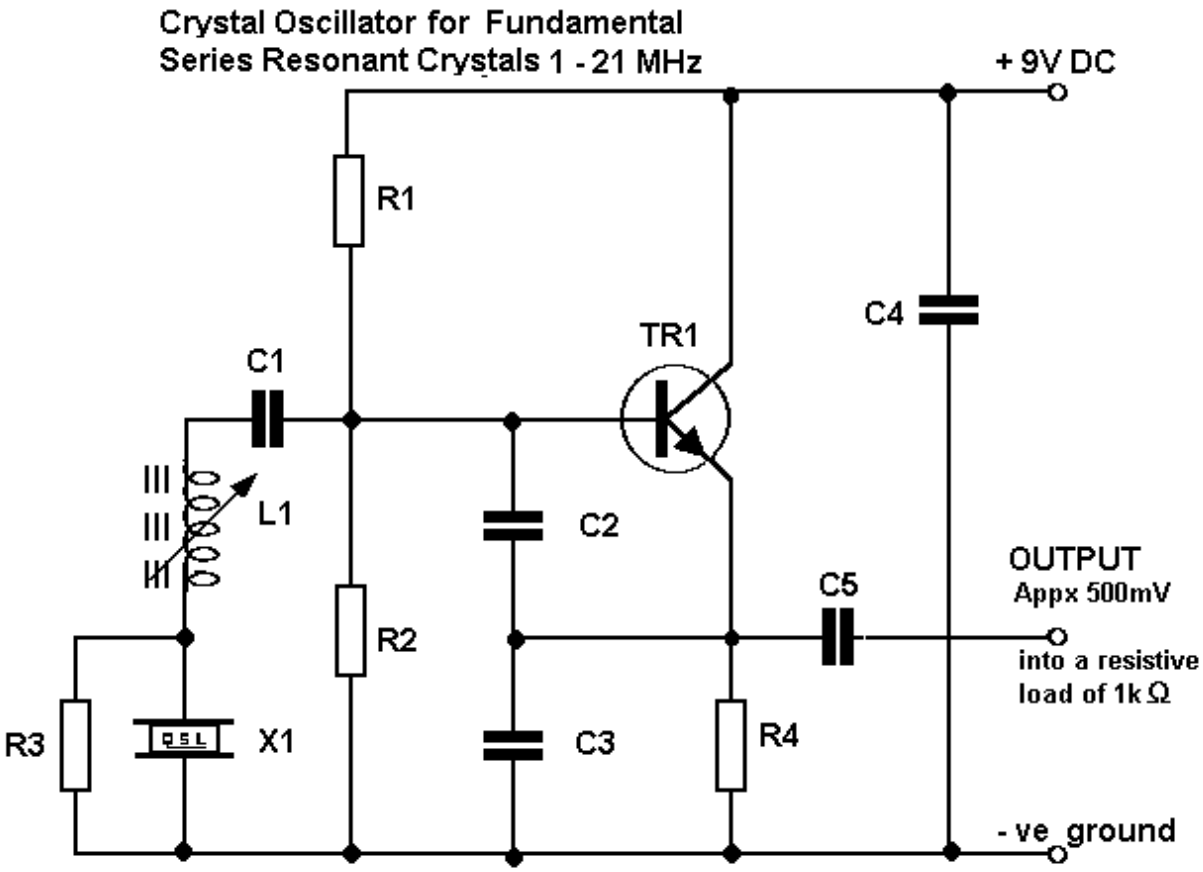
This side will explain some different Crystal Oscillators.

2.1.2.1 Introduction to Fundamental Crystal Oscillators 1 - 21 MHz

Crystal units manufactured by Quartslab Marketing Ltd for use over the frequency range 1 to 21 MHz use an AT cut quartz plate and operate in their fundamental mode. Crystal units may be specified for operation in either a series or parallel resonant condition. This operating condition should be correctly specified when ordering or the crystal unit will not operate on the correct frequency. Typically, over the frequency range of 1 - 21 MHz there may be between 2 and 15 kHz difference between the parallel resonant and series resonant conditions, the series resonant condition being lower in frequency.

If parallel resonance is required, it is necessary to specify a load capacitance for the Crystal. This capacitance is not related to any capacitance present in the crystals or the circuit but refers to the load capacitance used when crystals are measured in standard test sets. The preferred value of capacitance is 30 pF but crystals can be manufactured for other values.
These circuits are designed for non-critical adjustment and operation with easily available components. In each case, an output of at least 500 milli volts RMS is available across a load of 1000 ohms in parallel with 15 pF. The circuits are suitable for use with supply voltages from 5 to 10 volts DC. Over this voltage range frequency stabilities of 0.001% (10 ppm) should be achieved.
Please note that where no load capacitance is specified for fundamental crystals we supply them calibrated for a 30 pF load and although the circuit is shown as suitable for crystals at 0.95 MHz (950 kHz) we do not offer crystals below 1.5 MHz.

2.1.2.2 Series Resonant Circuit



R1, R2, R3, R4 See Below

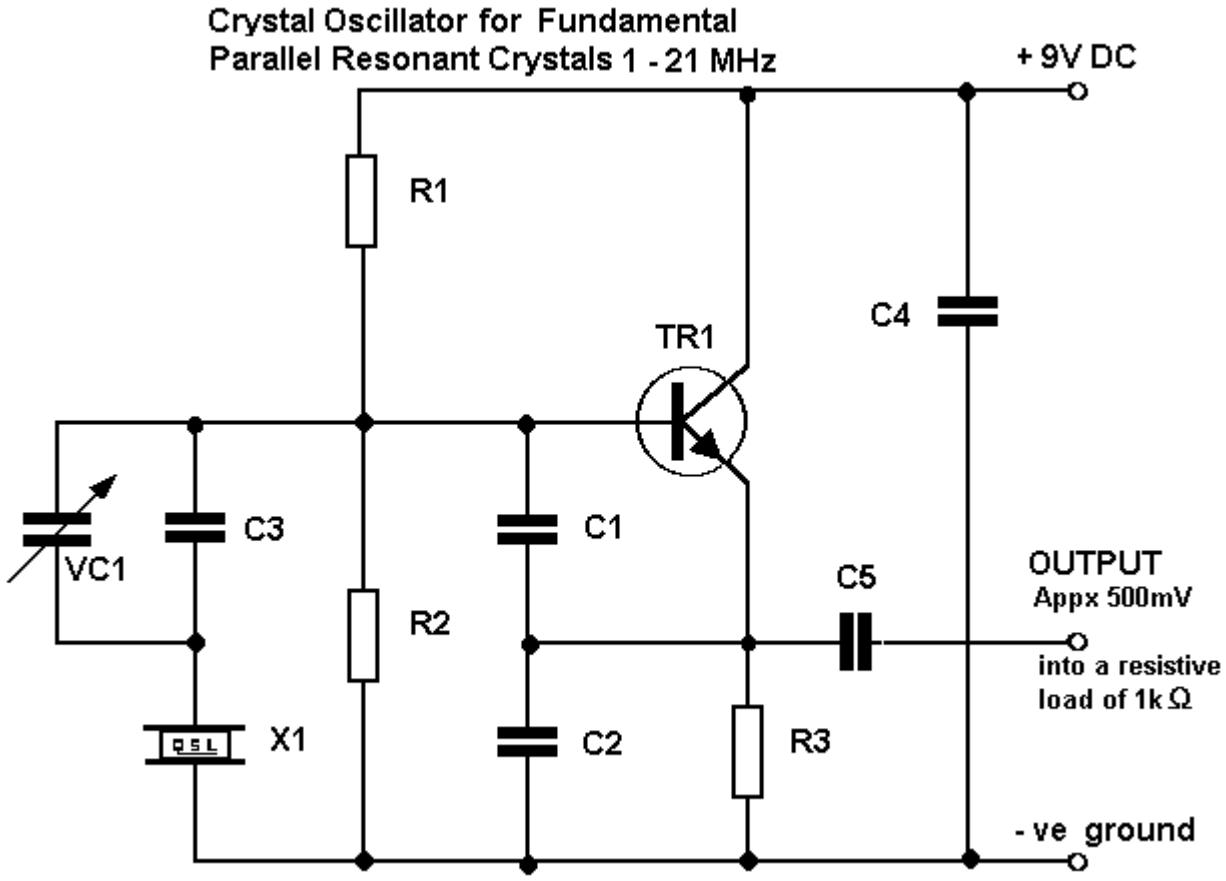
2.1.2.2.1.1 C1, C2, C3, See Below, C4 0.01µF, C5 47pF

TR1 BC108 or similar

L1 Close wound with 37SWG enamelled wire on 7.62mm diameter former with Neosid F25 coil

Frequency of X1 MHz	R1	R2	R3	R4	C1	C2	C3	L1
0.95 -1.65	68k	33k	*	2.2k	.0047mf	680 pF	680 pF	140 Turns
1.6 - 2.5	68k	33k	*	2.2k	.0047mf	680 pF	680 pF	65 Turns
2.5 - 4.0	68k	33k	560 ohm	1.5k	.0047mf	220 pF	220 pF	65 Turns
4.0 - 6.0	15k	6.8k	560 ohm	1.5k	.001mf	270 pF	270 pF	40 Turns
6.0 - 10.0	15k	6.8k	560 ohm	1.5k	150 pF	220 pF	220 pF	26 Turns
10.0 - 15.0	15k	6.8k	560 ohm	680 ohm	100 pF	220 pF	220 pF	16 Turns
15.0 - 21.0	15k	6.8k	560 ohm	680 ohm	100 pF	100 pF	100 pF	10 Turns

2.1.2.3 Parallel Resonant Circuit



R1 100K, R2 33K, R3 See below
C1, C2, C3 See below, C4 . 01µF, C5 47pF
VC 60pF Trimmer
TR1 BC108 or similar

Frequency of X1 MHz	R3	C1	C2	C3
0.95 -3.0	3.3k	220 pF	220 pF	not used
3.0 - 6.0	3.3k	150 pF	150 pF	33 pF
6.0 - 10.0	2.2k	150 pF	150 pF	33 pF
10.0 - 18.0	1.2k	100 pF	100 pF	not used
10.0 - 18.0	1.2k	100 pF	100 pF	not used
18.0 - 21.0	680 ohm	68 pF	33 pF	not used

2.1.3 Introduction to Overtone Crystal Circuits

With overtone operation of crystals, the overtone frequency is not an exact multiple of the fundamental frequency and the circuit design must ensure that the crystal does in fact operate at the overtone frequency.

In order to be certain of correct operation, it is preferable to specify series resonant crystals, and to provide external circuit elements to prevent oscillation at the fundamental frequency. Where parallel resonant overtone crystals are required a load capacitance must be specified

On following pages circuits are shown for 3rd overtone crystals 15 to 65MHz and 5th overtone crystals 60 to 105 MHz operating in their series resonant mode. In both of these circuits with the crystal short circuited, the oscillator should operate at or near the required frequency. With the crystal in circuit L1 should be adjusted for either (a) minimum voltage across the crystal or (b) for the exact frequency required. Ideally, these two points would coincide but they rarely will due to the need for a manufacturing tolerance on crystal frequency.

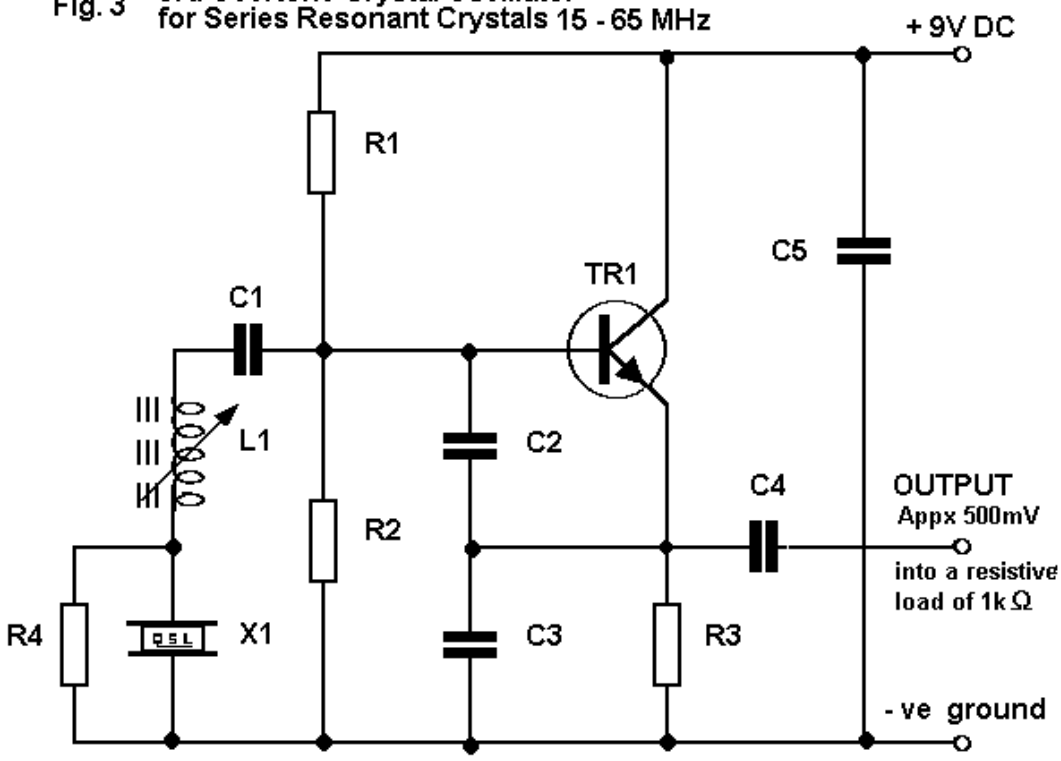
If L1 is of incorrect size it is possible for the oscillator to operate on a different order of overtone, for this reason it is important to accurately check the output frequency.

Under no circumstances should a tuned circuit at the crystal overtone frequency be included in the collector circuit of TR1 as this configuration will result in oscillation not controlled by the crystal. However it is possible to include a tuned circuit at that point which is twice or three times the crystal frequency. It is then possible to extract from the collector the harmonics of the crystal frequency.

Unless otherwise specified we supply 3rd overtone crystals between 21 and 60 MHz. 5th overtone between 60 and 126 MHz and 7th between 126 and 175 MHz.

2.1.3.1 Third Overtone Oscillator Circuit

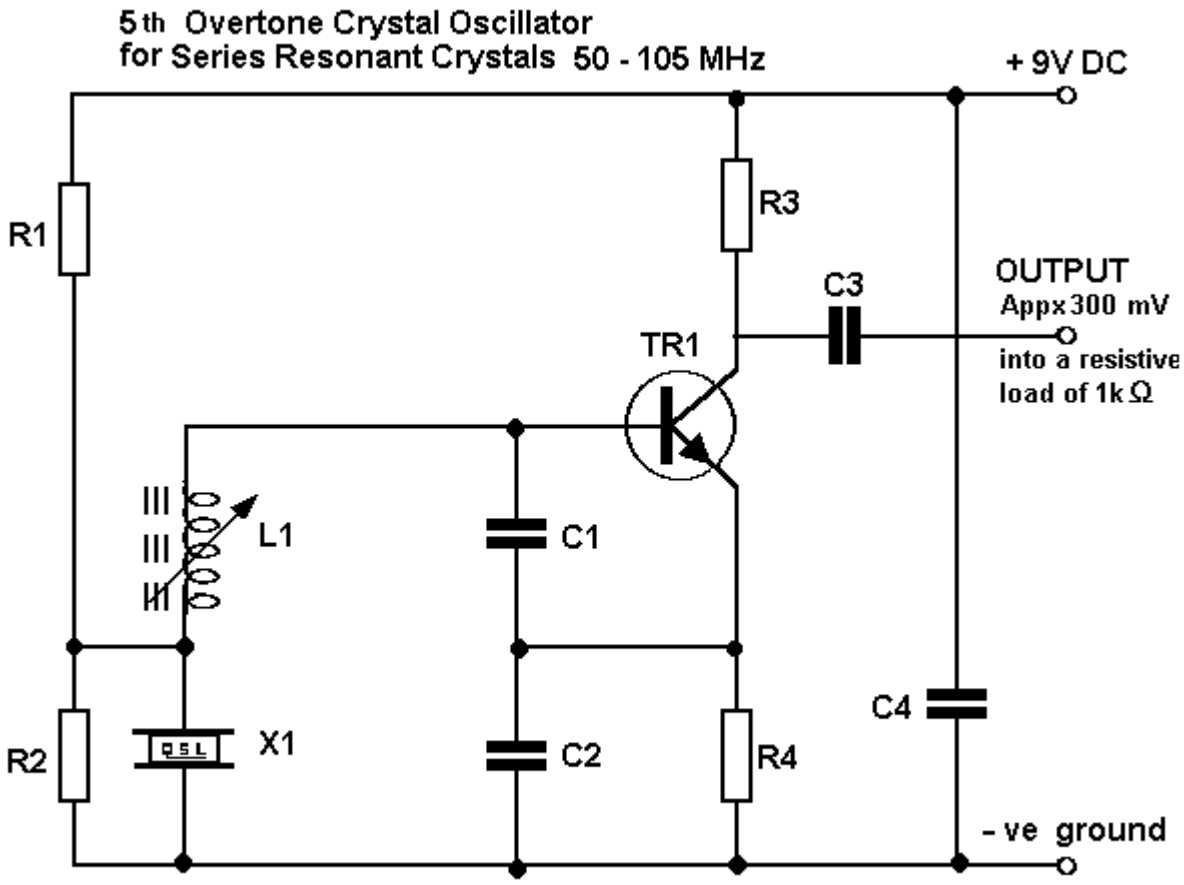
Fig. 3 3rd Overtone Crystal Oscillator for Series Resonant Crystals 15 - 65 MHz



R1 10K, R2 4.7K, R3 470 Ohm, R4 560 Ohm
TR1 BF180 or similar
C1 C2, C3, C4, See Below, C5 0.001mF
L1 wound is on a 7.62 diameter former with Neosid F29 core

Frequency MHz	C1	C2	C3	C4	L1
15 - 20	100 pF	100 pF	68 pF	33 pF	12 Turns 30SWG Close Wound
20 - 26	100 pF	100 pF	68 pF	33 pF	8 Turns 30SWG Close Wound
25 - 31	100 pF	68 pF	47 pF	33 pF	8 Turns 30SWG Close Wound
30 - 43	100 pF	68 pF	47 pF	33 pF	6 Turns 30SWG Close Wound
42 - 55	100 pF	68 pF	47 pF	33 pF	5 Turns 30SWG 6 mm long
48 - 65	68 pF	33 pF	15 pF	15 pF	5 Turns 30SWG 6 mm long

2.1.3.2 Fifth Overtone Oscillator Circuit



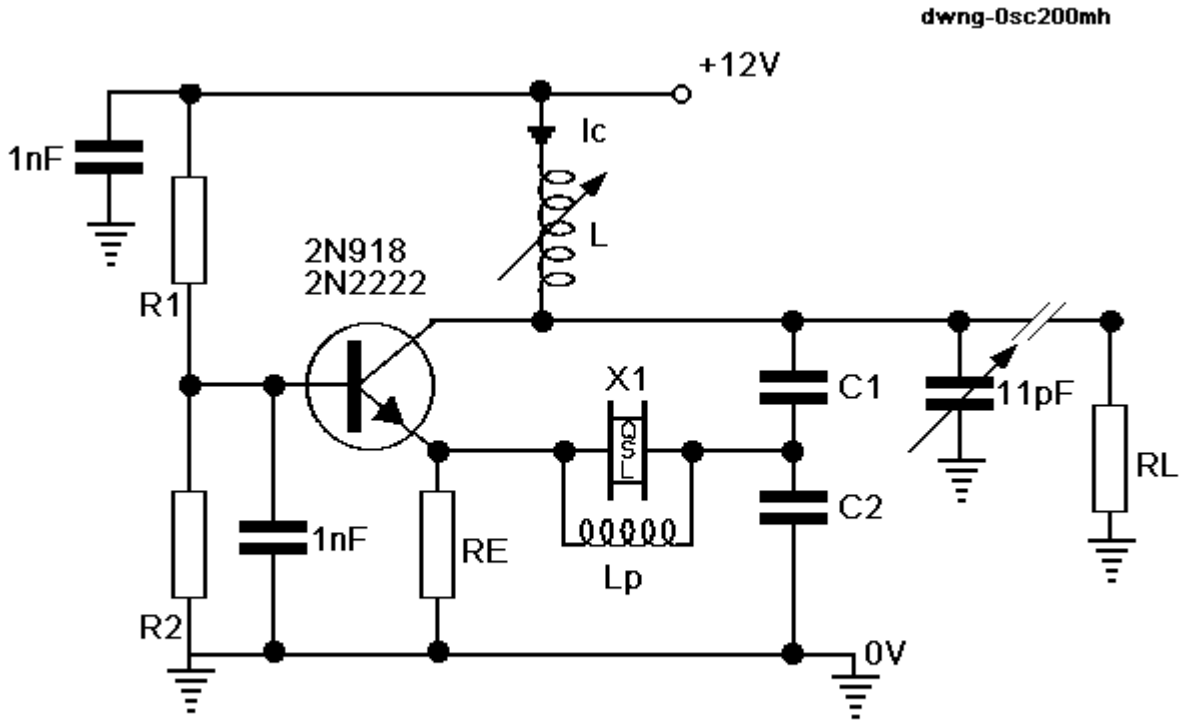
XL1 Ri L1
50-70 MHz 2.7 K 7 Turns 6mm long
60-85 MHz 2.7 K 5 Turns 5mm long
80-105 MHz 1.2 K 3 Turns 6mm long.

R2 470 ohm Cl l2pF
R3 330 ohm C2 18pF
R4 470 ohm C3 33pF
C4 1000 pF

VT1 8F180, SE1O1O or similar.
L1 Wound with 20 B & S enameiled wire on 7.62 mm diameter former with Neosid F29 Core.

Under no circumstances should a tuned circuit at the crystal overtone frequency be included in the collector circuit of VT1, as this configuration will result in oscillation not controlled by the crystal.

2.1.3.3 OVERTONE CRYSTAL OSCILLATOR FOR UP TO 200 MHz



Overtone Oscillator up to 200 MHz

Frequency	C1	C2	Ic (mA)	RE (Ohms)	RL (Ohms)	Lp (mH)
75	8 pF	100 pF	25	510	470	0.25
120	8 pF	50 pF	25	390	300	0.1
150	5 pF	25 pF	5	1.1k	600	0.08
200	3 pF	20 pF	5	1.1k	600	0.05

The above diagram shows a true series resonant oscillator circuit suitable for use up to 200 MHz

It is recommended that transistors for use in this circuit have a high DC gain (HFE) and a low base resistance (RBB). Also ensure that the transit frequency is at least ten times that of the oscillator frequency.

2.2 Osciladores controlados por voltaje.(VCO).(1.1)

2.2.1 Tracking Advances In VCO Technology

Tracks the history of voltage-controlled oscillators (VCOs) since approximately 1910. Provides examples of VCO integration in RF ICs. Presents technology, performance and size evolution to the present date. Based on history and technology, future trends are projected.

Voltage-controlled oscillators (VCOs) are commonly found in wireless systems and other communications systems that must tune across a band of frequencies. VCOs are available from a wide range of manufacturers in a variety of package styles and performance levels. Modern surface-mount and radio-frequency-integrated-circuit (RFIC) VCOs however, owe their heritage to engineering developments that began almost a hundred years ago. Improvements in VCO technology have continued throughout that time, yielding ever smaller sources with enhanced phase noise and tuning linearity.

Oscillators have been essential components from the time Edwin Armstrong discovered the heterodyne principle1. In this application, an oscillator feeds sinusoidal signals to a nonlinear mixing element to effect frequency translation by multiplying the oscillator's signals with other input signals. Of course, Armstrong realized that what he needed to control the frequency translation was an electrical circuit which produced a stable sinusoidal time-varying voltage (or current) with a corresponding frequency. He discovered around that same time that an Audion (an early vacuum tube) could be configured to produce an oscillation, and he effectively devised the first electronic oscillator2 (rather than the crude spark-gap oscillators used in early wireless transmitters).

In retrospect, Armstrong started a revolution in oscillator technology that quickly made spark transmitters obsolete, leading to the development of high-performance radio receivers. From the time of Armstrong's discoveries in the 1910's to the modern era, VCO technology has progressed from vacuum tube oscillators to transistor oscillators to oscillator module solutions and finally to today's RFIC-based oscillators. The face of VCO technology is again rapidly changing and soon in many systems will only resemble early oscillators in basic topology and/or mathematically.

Armstrong's discovery was soon improved upon by Rober V.L. Hartley, with the invention of his oscillator circuit topology (Figure 1). Hartley made use of improvements in vacuum-tube technology and devised a oscillator circuit in which the vacuum tube acted as an amplifying device with inductive feedback applied to create a regenerative oscillation. The frequency of oscillation was established by the coil inductance and the circuit capacitance. This circuit was a breakthrough in the generation of a sinusoidal signal; it provided a much greater range of possible frequencies simply by varying the value of the coil or capacitor. The Hartley oscillator circuit was popular in transmitters and was quickly adapted for use in World War I. Both transmitters and receivers made use of the new tube-based oscillators circuit. Oscillator circuit innovations proliferated, giving rise to the predominant circuit topologies still in use today, such as Hartley, Colpitts, Clapp, Armstrong, Pierce, and other topologies.

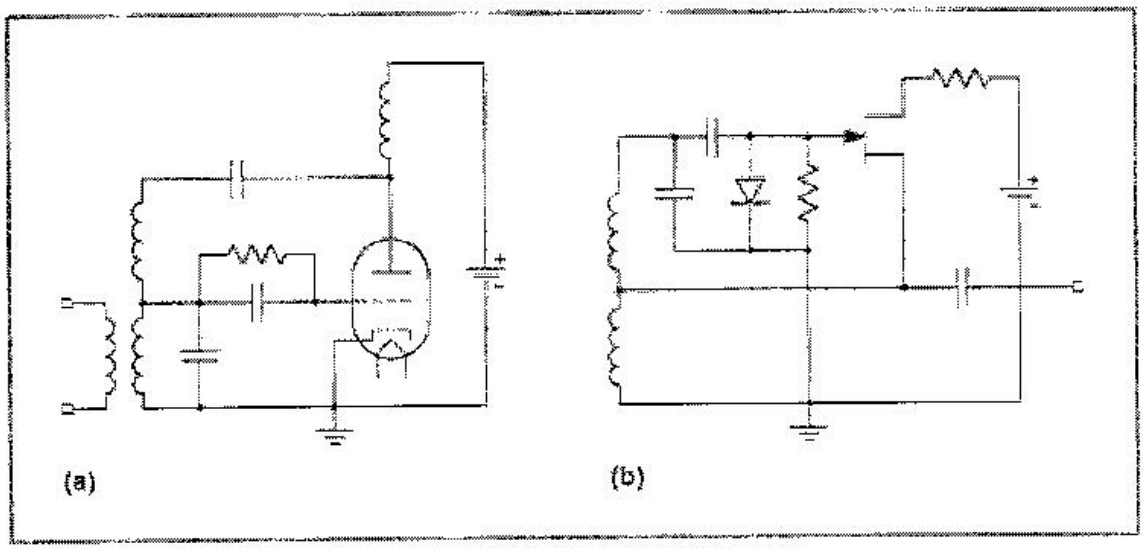


Figure 1. Examples of the Hartley oscillator; (a) triode implementation (b) JFET implementation

In Armstrong's superheterodyne receiver principle, input signals are mixed with oscillator signals to produce a constant intermediate frequency (IF). To maintain the constant IF, the oscillator must change frequency as the input signals change frequency. With a variablefrequency oscillator is was possible to tune the frequency translation circuit to a wide range of input RF signals and therefore enable multichannel communications, such as amplitudemodulated (AM) radio. Such variable-frequency oscillators were an adaptation of the basic resonant-circuit oscillators, in which one of the resonant elements (an inductor or capacitor) would vary. Most often, it was the capacitor that was varied. High-quality variable capacitors were constructed from ganged multi-plate metal air-gap capacitors. As radio technologies advanced, a tremendous amount of innovation took place in the implementation of oscillator circuits. Engineers devised countless types of coils, variable capacitors, feedback techniques, and vacuum tubes to implement oscillator and frequency-conversion circuits.
Many elaborate and elegant schemes were devised to provide precise, high quality tuning of the oscillator frequency via a mechanical dial on the front on the radio. Figure 2 is a picture of a re-created vintage 1929 Hartley style transmitter (as re-creaed by Ham radio enthusiast W9QZ). Like many early implementations of electronics, the circuit was bulky and expensive and required high supply voltages.

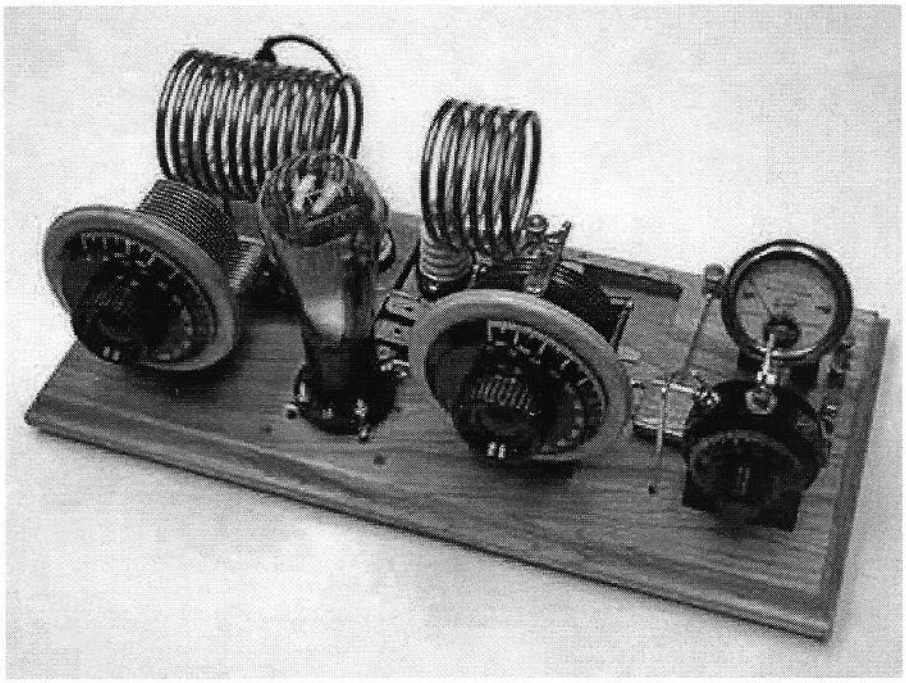


Figure 2. Vintage 1929 Hartley style transmitter

The vacuum-tube oscillator was widely employed for many years in commercial and military radio receiver applications, such as AM and frequency-modulated (FM) radios, television, and military voice communications. However, the discovery of semiconductor amplifying devices, such as the transistor and the varactor diode, led to the next dramatic change in VCO technology. The first bipolar transistor was discovered in the late 1940's at Bell Laboratories (Holmdel, NJ), and transistors became available in the 1950's as replacements for vacuum tubes. The new transistors were smaller and consumed less power than tubes, with lower operating voltage requirements and ultimately lower cost. The transistor became a replacement for the vacuum tube as the active element in oscillators and significantly changed the practical implementation established oscillator topologies.

Arguably, the introduction of the varactor diode (with a voltage-variable capacitance arising from a reverse-biased PN junction) had a greater impact on the direction of VCOs than the transistor. In the early 1960's, a great deal of research was performed on varactor technology, and varactors rapidly displaced mechanically adjustable components as the variablecapacitance element in VCOs. Varactors proved invaluable in the development of phaselocked- loop (PLL) circuits for precise electronic control of frequency sources. The rapid growth of television during that time contributed greatly to the migration to varactor- and transistor-based VCOs. Cost-effective, low-power, high-quality VCOs with inherent electronic tuning and easily reconfigurable frequency ranges were now possible. Discrete-transistor and varactor-based VCOs dominated electronic designs of the 1960's through 1980's. But, in the 1980's two new technologies impacted VCO developments: modular approaches and monolithic VCO integrated circuits (ICs). Figure 3 shows a timeline illustrating the development of VCO technologies over the past 80 years.

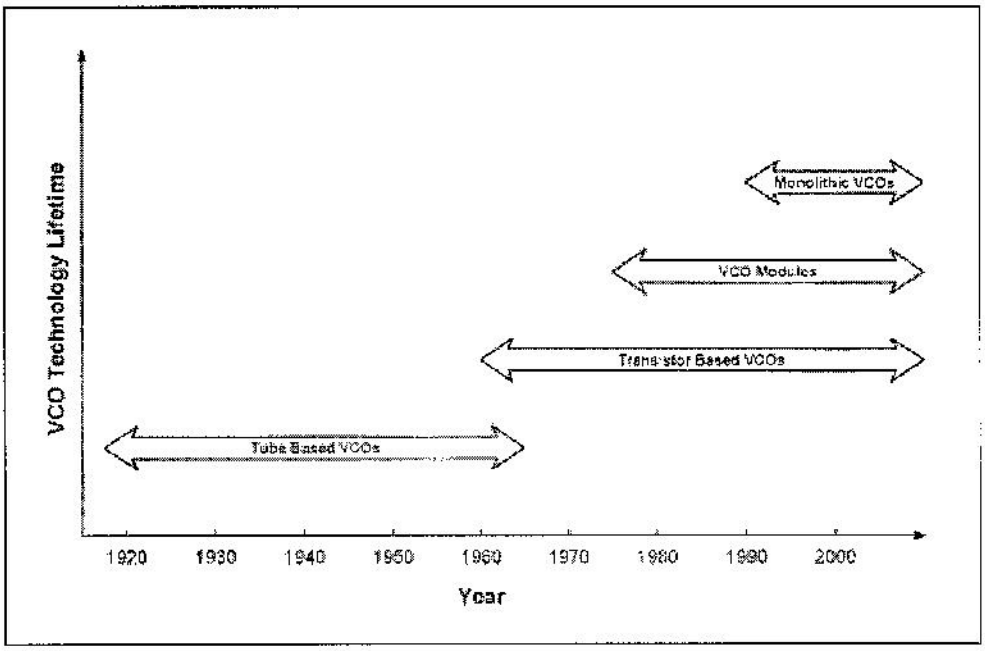


Figure 3. Chart of VCO technology lifetimes versus year

The shrinking sizes of varactors, capacitors, and inductors made possible VCOs in module form. A VCO module is essentially a miniature version of a discrete-component oscillator constructed on a substrate that is mounted into a metal housing. The module is self-contained and requires only connections to ground, the supply voltage, the tuning voltage, and the output load. Such modules first appeared in the 1960's primarily for military applications. They were fairly large (several square inches) and relatively expensive. Discrete transistor and varactor implementations of VCOs were still used in commercial products. It was not until the emergence of mobile telephony that a commercial market emerged for VCO modules.

Although discrete VCOs could be custom designed to any frequency and tuning range, they typically required labor-intensive production adjustment of the frequency-setting elements to compensate for component variations. In addition, discrete VCOs needed good shielding to minimize emissions and reduce pulling effects. But with the growing sales of mobile telephones in the late 1980's and early 1990's, demand increased for "canned" oscillator modules. Some Japanese companies, being increasingly proficient in miniaturization, developed small, cost-effective VCO modules for mobile telephones. As new wireless application arose, VCO module manufacturers developed products with frequency plans unique to each application. As surface-mount components became progressively smaller (1206, 0805, 0603, 0402, 0201), new smaller, lower cost VCO modules were developed. Figure 4 illustrates the size reduction over time of the "typical" state-of-the-art commercial VCO module. Today, these improvements have culminated in compact (4 x 5 x 2mm) modules that sell for close to $1.00 (US) in high volumes. This 15 year cycle of shrinking VCO module volume was a truly amazing reduction in size and satisfied the tough space constraints imposed by the new mobile wireless devices, such as cellular phones. Yet, an even smaller and more cost-effective VCO technology would emerge by the end of the 1990's; monolithic VCO IC technology.

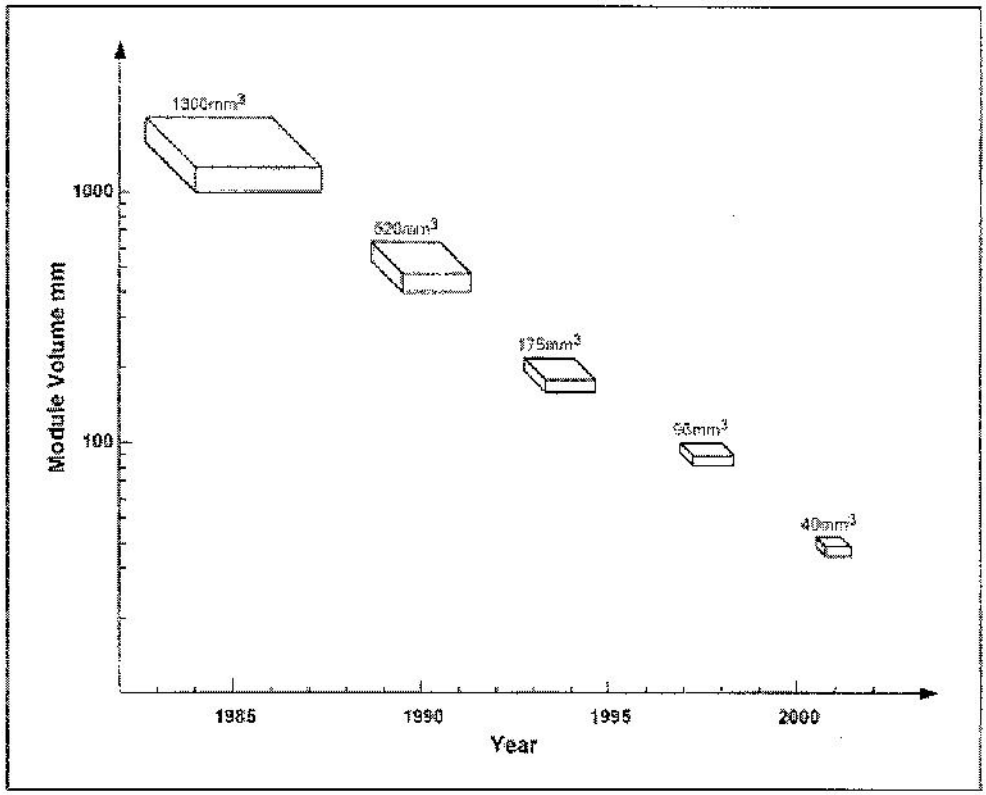


Figure 4. VCO module size scaling versus time

Monolithic IC VCO technology is defined as a VCO implementation in which all the circuit elements of an LC VCO: transistors, capacitors, resistors, inductors, and varactor diodes; are integrated on one chip. As in a VCO module, the devices are configured to form a complete VCO, requiring only connection to the power supply, ground, output, tuning input and any digital control lines. (Note that voltage-controlled ring oscillator circuits have been excluded from this definition of VCOs, given that their phase noise is much poorer and eliminates its use in most radio systems.) The first instance of a monolithic VCO IC coincided with the development of Gallium Arsenide (GaAs) IC technology and monolithic microwave integrated circuits (MMICs). The monolithic VCO emerged in the literature [1,2] in the early 1980's during a period of intense research into commercial and military applications for MMICs (funded largely by the US DARPA MIMIC program). Early MMIC VCOs were fabricated with GaAs IC processes, using 2-in.-diameter wafers, although the MMIC VCOs were not particularly area efficient and therefore were not cost effective. Generally, these VCOs operated at multi-GHz frequencies consistent with the target applications, satellite receivers and radar systems.

Most of the early monolithic GaAs VCOs were developed as part of the DARPA MIMIC research, with little impact on commercial markets. Silicon IC technology was still relegated to low frequencies during the 1980's, and lacked the bandwidth needed for gigahertz-frequency monolithic VCOs. But by the 1990's, silicon IC technology had been developed with sufficiently high transition frequencies (fT) and suitable monolithic components (high-Q inductors and high-frequency capacitors and varactor diodes) to enable development of higherfrequency silicon monolithic VCOs. And wireless markets had emerged with sufficient

size and growth potential to spur the demand for low-cost VCOs in the 800 to 2500MHz bands.

Prior to this, most commercial radio systems operated at frequencies sufficiently low as to make construction of a monolithic VCO IC impractical; on-chip inductor values were simply too large. The first apparent instance of a silicon monolithic VCO IC in the literature is from the University of California at Berkeley in 19923. The VCO employed a unique, unorthodox topology in which the frequency was varied by electrically "interpolating" between two separate resonant circuits, even though it was still technically an implementation of monolithic silicon VCO IC technology. Arguably, this work and further research by Professor Robert Meyer and his graduate students at the University of California at Berkeley appears to have ushered in a period of increased research on monolithic VCOs.

By 1995, work on silicon monolithic VCO ICs was being reported in the technical literature by researchers at leading universities4,5. In these reports, researchers disclosed some of the first examples of modern, monolithic LC (inductance-capacitance) resonator VCO ICs. In 1996 to 1997, a tremendous number of papers appeared describing work on different implementations of monolithic VCOs6-12. This period effectively marked the emergence of the commercially viable monolithic VCO ICs. The monolithic VCO ICs were being developed in both high frequency bipolar transistor IC technology and silicon CMOS IC technology. Academic researchers typically used CMOS technologies to take advantage of the widespread availability of the IC technology, while industrial researchers used RFIC-specific bipolar/BiCMOS process technology. Figure 5 shows a typical monolithic VCO circuit implemented in both CMOS and bipolar/BiCMOS process technology.

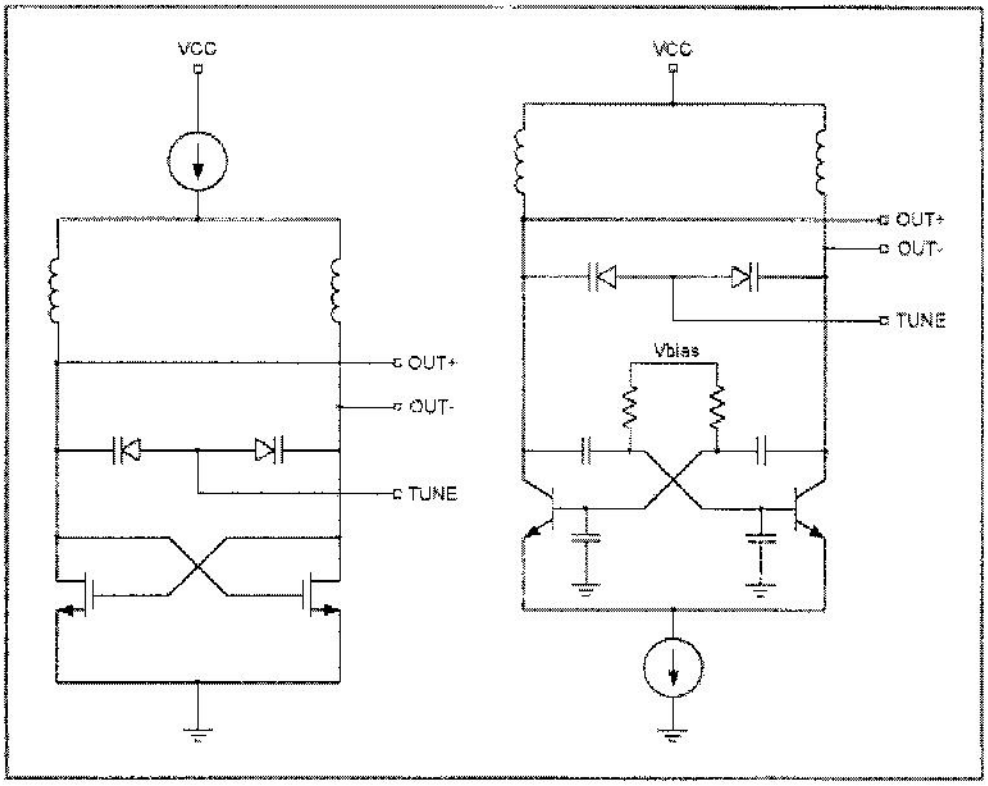


Figure 5. Typical monolithic VCO core circuit in MOS and bipolar

Generally, the overall performance of these early VCO IC implementations was inferior to discrete implementations and VCO modules. Specifically, the phase noise and tuning characteristics were poorer than what could be routinely achieved in discrete designs or VCO modules. This shortfall was principally due to the low Q inductors and crude varactor diodes commonly available in that generation of IC technologies.
However, monolithic VCOs proved to be extremely small, cost-effective, and available in the same process in which RF transceiver functions were being implemented. This meant that the VCO could be integrated with other RF and IF functions, such as the mixer, low-noise amplifier (LNA), and phase-locked loop (PLL). This capability to cost-effectively integrate the VCO with other receiver and transmitter functions helped make the monolithic VCO IC a commercial reality. A good early example of this was a commercial 900-MHz spread-spectrum cordless-telephone chipset13.
In the late-1990's, research on VCO IC technology intensified considerably14-20. This was in large part due to the explosion in the wireless markets and also in the proliferation of high frequency bipolar, CMOS, and BiCMOS process technologies. Significant research and development took place at both industrial and academic levels. Researchers focused on improving the phase-noise performance, extending the frequency of operation and adjustment of the VCO's tuning range on-chip. useful improvements in performance. These improvements achieved electrical specifications which permitted the VCOs to be use in RFICs for cordless phones, Bluetooth, WLAN , GPS and DBS applications. Table 1 shows a summary of some commercial RFICs which contain monolithic VCOs.

Table 1. Examples of monolithic VCOs integration in commercial RFICs

Unit	FrequencyRange	Source	Application
MAX2622-24	855-998MHz	Maxim	general purpose 900MHz ISM
MAX2750-53	2025-2500MHz	Maxim	general purpose 2.4GHz ISM band
MAX2754	1145-1250MHz	Maxim	2.4GHz cordless phones
MAX2115	925-2175MHz	Maxim	DBS
MAX2900	902-928MHz	Maxim	900MHz ISM band (wireless meter reading)
MAX2820	2400-2500MHz	Maxim	802.11b WLAN
RF105	902-928MHz	Conexant	900MHz cordless phones
SA2400	2400-2500MHz	Philips 802.11b WLAN	
BlueCore-01	2400-2500MHz	CSR	Bluetooth
TRF	2400-2500MHz	TI	Bluetooth
GRF2i/LP	1575MHz	SiRF	GPS
AR5111	5.2-5.8GHz	Atheros	802.11a WLAN

These VCO ICs and the integrated solutions that contain them are smaller and more cost effective than VCO modules and easier and faster to apply than discrete solutions. The monolithic VCOs provide significantly improved value over previous technologies. The performance of this generation of VCO technology is sufficient for systems like cordless phones, wireless data radios and DBS receivers; and therefore is being widely adopted for

use in these systems. However, the phase-noise performance is presently insufficient (the noise is about 5 to 10dB too high) to meet the requirements of higher-date-rate mobile telephone systems (such as GSM, IS-136, CDMA, etc). Low inductor Q and excess bias noise contribute to limits for the VCO phase noise. Although some researchers had demonstrated promising results with the use of bond-wire inductors, low phase-noise performance has remained elusive and out of reach of monolithic VCO IC technology. However, this is appears to be only temporary. In the last three years (1999-2001), many significant advances in VCO design have been reported and point out some clear trends for the future.

2.2.1.1 Major Trends

Several trends are impacting the development of monolithic VCOs with improved phase noise. For example, basic RFIC process technologies are improving. The quality factors possible with semiconductor processes is increasing, and the performance of active and passive devices is improving. Even with silicon processes, transistors can now be fabricated with fT performance exceeding 50GHz, and higher-Q varactor diodes are available with wide capacitance ratio tuning ranges (low series resistance). These processes feature lower-loss substrates with thicker metalizations and higher-Q inductors. The processes are capable of devices with reduced parasitic elements, leading to VCOs with lower phase noise, higher operating frequencies, and lower-current operation.

Design techniques are also becoming more advanced. VCO researchers are exploiting the power of IC technologies by devising more sophisticated circuits to improve performance. These researchers are introducing techniques previously impractical with discrete VCO or module VCO implementations, such as differential oscillator topologies, amplitude control, second-harmonic traps, IC transformers for improved coupling, topologies with multiple oscillators, and architectures capable of higher-frequency operation.

Design engineers are also gaining a better understanding of VCO theory. They are building upon mathematical models from the past, such as Van der Pol's and Lesson’s equations, and devising new analytic expressions for oscillator behaviour (such as tuning characteristics and phase-noise performance). For example, designers are on the cusp of amending Lesson’s noise equations with Abidi's relationships. In addition, computer-aided-engineering (CAE) tools are growing in power and sophistication as the processing capabilities of personal and workstation computers increases, allowing engineers to experiment with VCO behavioural models to discover performance enhancements.

Monolithic VCO technology continues to appear in an increasing number of new products, with high-quality VCOs integrated with the transceiver circuitry. For example, the latest transceivers for the WLAN and Bluetooth markets integrate the VCO within the RF transceiver IC, resulting in a dramatic reduction in size compared to discrete components. In higher performance WLAN radios (2.4-GHz IEEE 802.11b and 5-GHz 802.11a versions), system requirements call for higher-performance VCOs with the very low phase noise needed to achieve the needed packet data rates and blocking performance levels. Improvements in RFIC VCO technology make these integrated sources ever more attractive for an increasing number of commercial RF applications, including satellite receivers, CATV set top boxes, wireless data applications, cordless telephones, and mobile telephones. Clearly, monolithic VCOs are winning an ever-increasing share of high-volume applications compared to discrete and module VCO solutions. The time is coming very soon when monolithic VCOs will be the

dominant oscillator approach in all high volume commercial wireless systems. VCOs have traversed a remarkable path from bulky tube based circuits to <1mm sq of silicon.

2.2.1.2 References

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Notes

1 The heterodyne principle is defined as the multiplication of two signals in the time domain in order to produce a frequency shift in the frequency domain. The principle is the fundamental basis for frequency translation of signals in wireless systems.

2 Both Edwin Armstrong and Lee DeForest were working on regenerative receiver circuits at the time. These regenerative circuit created the first oscillators. A similar version of this article appeared in the July 2002 issue of *Microwave and RF* magazine.

MORE INFORMATION ON: MAX2622, MAX2624, MAX2750, MAX2753, MAX2754, MAX2820 AND MAX2900, search the Maxim Web site.

2.2.2 THE DESIGN PRINCIPLES OF VOLTAGE CONTROLLED OSCILLATORS

What exactly is a voltage controlled oscillator or as more commonly known a vco?, what is its purpose in life?

2.2.2.1 A PRACTICAL EXAMPLE

Here I'm going to use a very practical example where one of my readers has a requirement for a voltage controlled oscillator operating at 1.8 - 2.0 Mhz (amateur radio band 160M). This is to be part of a frequency synthesiser, although a vco isn't always associated with a frequency synthesiser.

The very high costs and difficulties encountered when buying quality variable capacitors today often make vco's an extremely attractive alternative. As an alternative all you need is an extremely stable BUT very clean source of dc power, a varactor diode and a high quality potentiometer - usually a 10 turn type. Please note that circuit Q tends to be somewhat degraded by using varactor diodes instead of variable capacitors.

For people who are confused at this point allow me to explain. Diodes when they have a reverse voltage applied exhibit the characteristics of a capacitor. Altering the voltage alters the capacitance. Common diodes such as 1N914 and 1N4004 can be used but more commonly we use varactor diodes specifically manufactured for vco use e.g. Motorola's MVAM115, Philips BB112 and BB212. They are also sometimes called tuner diodes.

The design requirements asked for were:-

- (a) frequency coverage 1.8 - 2.0 Mhz
- (b) voltage controlled by a frequency synthesiser with an output level sufficient to drive the input of a Phase Locked Loop (PLL)
- (c) a further buffered output for a digital frequency readout.
- (d) another buffered out put to drive succeeding amplifier stages.

Because in this example the ultimate frequency stability is determined by the reference crystal in the frequency synthesiser there can be some relaxation of stability standards. The buffered outputs will be covered under buffer amplifiers.

Let's look again at our previous oscillator circuit. If you are unfamiliar with oscillators then review my previous oscillator tutorial. It will certainly help you.

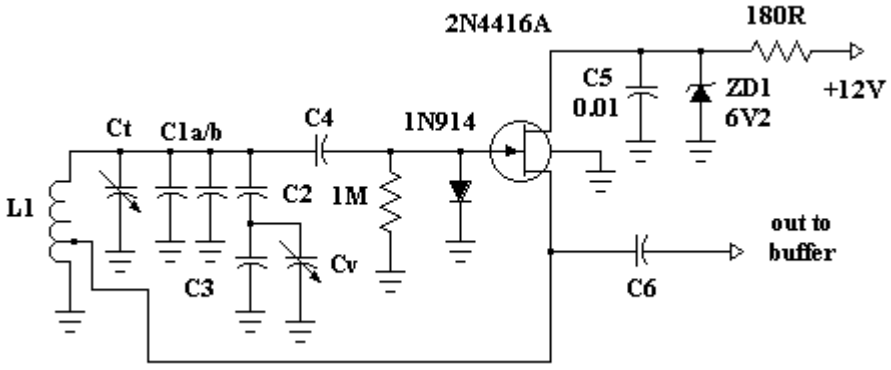


Fig 1.

2.2.2.2 VARACTOR DIODE

Here Cv the variable capacitor, could be replaced by a suitable varactor diode as a tuning diode and in actual fact our reader has on hand a Motorola MVAM115 varactor. This I think is nearly similar to my Philips BB112 diode. So we will rehash the above figure 1 to acomodate varactor diode tuning instead of using a conventional variable capacitor.

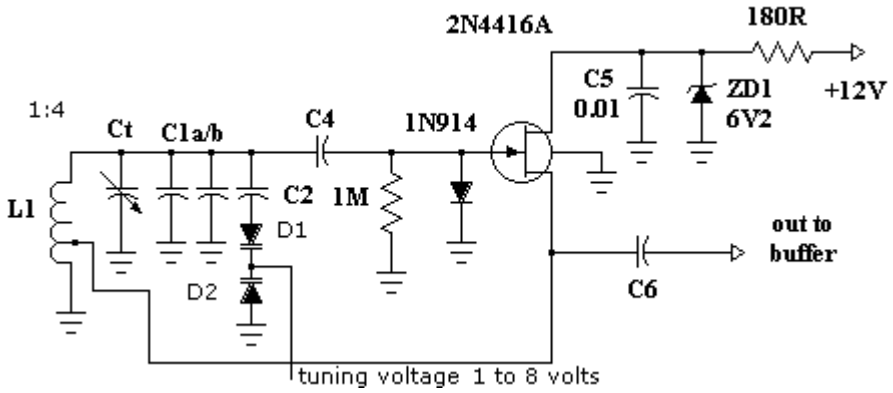


Fig 2.

Now I've left Ct and C1 a/b all in the circuit. In this application of a frequency synthesiser they are unlikely to be necessary. To tune from 1.8 to 2.0 Mhz which is a frequency swing of 2 / 1.8 = 1.111 - which when squared means we need a capacitance ratio of 1.234 to 1
That means the ratio of minimum combined capacitance in the circuit to maximum combined capacitance in the circuit must change by 1.234 to 1.
Looking back at the tutorial on oscillators I said the inductor should have a reactance of about 180 ohms. So around the frequency of interest I expect an inductor of about 15 uH to be used for L1 in Fig 2.
You should be used to calculating LC numbers by now but L X C at 1.8 Mhz = 7818 and at 2 Mhz it works out about 6332. Dividing both by our 15 uH inductor we get a Cmin of 422 pF and Cmax of 520 pf. Which incidentally if you check 520 / 422 = 1.232:1 So the variation of C is 520 - 422 = 98pF swing.
For synthesisers or any voltage tuning you should have the largest voltage swing possible. This minimises the effects of noise voltage on the tuning voltage. My BB112 diode can be operated ideally from 1V to 8V. That means we can tune the 200 Khz (2.0 - 1.8) with a variation of 8 - 1 = 7 volts. It follows 7v / 200 Khz = 35 uV/Hz. If our noise level is below this then the tuning can't be varied or fm'ed by noise.
At 8V my diode exhibits a capacitance of around 28 pF while at 1V the capacitance is about 500 pF. If Mr. Philips answered my emails I could possibly reproduce here for you the capacitance versus voltage graph which would be helpful. Hullo anybody with authority from Philips or Motorola reading this - hint, hint. Help always welcome.

2.2.2.3 DIODES BACK-TO-BACK

You will note I have two diodes back-to-back in series in Fig 2. Although this in effect divides total varactor diode capacitance by two it eliminates the nasty effect of the rf present in the tank circuit driving a single diode into conduction on peaks which will increase the bias voltage, this also gives rise to harmonics.

It follows that my varactor diode capacitance now swings a net approximate 14 pF up to 250 pF when the bias voltage is varied from 8 volts down to 1 volt. You can of course go below 1V for higher capacitance but I tend to be conservative and generally do not go below 1V very much.

Now we have a net swing of 250 - 14 or 236 pF. You will recall above I said "the variation of C is 520 - 422 = 98pF swing" so how do I reduce a 236 pF swing down to a 98 pF swing? Look at capacitor C2 which is in series with both varactor diodes, does this not reduce the net capacitance?

2.2.2.4 CALCULATING NET CAPACITANCE

This is a simple mathematical problem (Oh God - not again). In this case we can use the formula C2 = [(Ca * Cb) / (Ca - Cb)] where Ca = existing C or in this case 236 pF and Cb = desired C or 98 pF. Now this isn't terribly accurate but you finish up in the ball park. Plugging those numbers into our sums we get C2 = [(235 * 98) / (236 - 98)] or 23030 / 137 = 168 pF. Bearing in mind with a vco and the voltage swings involved, you can get a fair bit of leeway and that each varactor diode varies greatly from predicted data of capacitance versus voltage. That means a lot of this is guesswork or suck-and-see. Technically it means it's all determined "empirically". All of that just says we will use a 180 pF capacitor for C2.

Using a 180 pF capacitor for C2 and putting it in series with D1 and D2 we get at 1 volt D1 = 500 pF, D2 = 500 pF and C2 = 180 pF. Net result = 1 / [(1 / 500) + (1 / 500) + (1 / 180)] which is about 105 pf.

Similarly at 8 volts we get D1 = 28 pF, D2 = 28 pF and C2 = 180 pF. Net result = 1 /[(1 / 28) + (1 / 28) + (1 / 180)] which is about 13 pf.

It follows the swing now becomes 13 pf to 105 pF or a net 92 pF which is near enough for this exercise. I had said very much earlier "by using our 15 uH inductor we get a Cmin of 422 pF and Cmax of 520 pf. Which incidentally if you check 520 / 422 = 1.232:1 So the variation of C is 520 - 422 = 98pF swing". How do we get near this requirement?

If we need Cmax of 520 pF and our series connection gives us 105 pF we need an extra 520 - 105 = 415 pF. On the other hand Cmin required is 422 pF and the series connection provides 13 pf we need 422 - 13 = 409 pF. It can be seen if we allow a trimmer of say 25 pF for Ct, which is the suggested trimmer in figure 2 - (that is Ct can varied from say 5 to 25 pF) - and we allow the combination C1 a/b to be a total of around 390 pF we have obviously achieved our goal. Is this not cool?

For our inductor L1 I would use a toroid although if you have access to a variable inductor you could use it. An air cored inductor most likely would be too large to consider. Suitable toroids of the Amidon / Micrometals type would at 2 Mhz be the T50-2 type which would require about 55 turns of #26 wire or even the T68-2 type requiring about 51 turns of #24 wire. Both gauges mentioned are those which will conveniently fit around the core.

No matter your frequency range of interest the basic principles outlined above will more or less still apply.

2.2.2.5 TUNING DIODE VOLTAGE

For a frequency synthesiser the tuning voltage is derived from the low pass filter of the PLL and you don't need to worry about it. On the other hand when you have an application of replacing a variable capacitor and manually tuning with say a ten turn potentiometer you need to be very careful about the "quality" of the voltage. It MUST be clean!
Below in Figure 3 is a suggested schematic for deriving suitable tuning voltages.

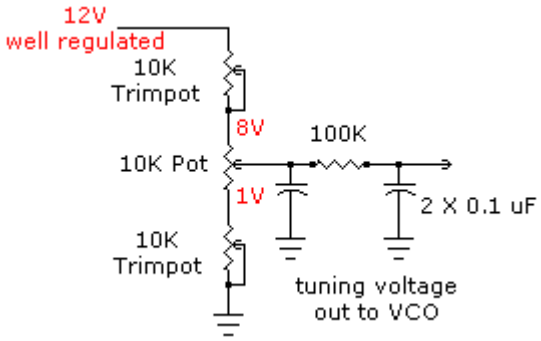


Fig 3.

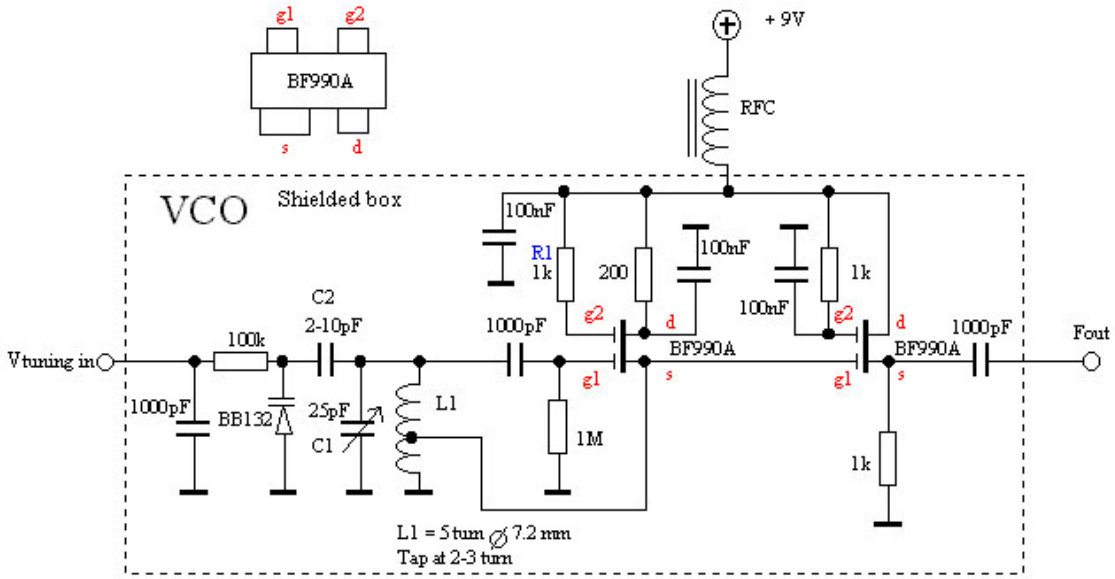
The 10K pot is your 5 or 10 turn "quality" potentiometer for tuning, the upper and lower trim pots (set and forget) allow you to adjust the voltage range of your choice that your tuning potentiometer will see. Again use "quality" trimpots. The 100K resistor and the two 0.1 uF capacitors are further filtering. Obviously there is considerable interaction between the trimpots and potentiometer so expect a lot of juggling back and forth.
If you wished, in some applications, both trimpots could be replaced by fixed resistors. It is simply a matter of using ohms law.

2.2.3 VCO-Voltage Controlled Oscillator

This side will explain a VCO based on Hartley oscillator. The VCO is easy to build and easy to adjust. The VCO below can be adjusted from 70-210 MHz.

Function

The VCO is based on a Hartley oscillator. The frequency is determined by L1 and capacitor C1. The V tuning voltage will change the capacitance in the varactor BB132 which will change the oscillation-frequency. The value of capacitor C2 will determine how much the frequency can be changed by the tuning voltage. The larger value the more the frequency will change. This VCO is based on two dual-gate FET. First FET is a Hartley oscillator where the frequency is determined by the value of L1, C1, C2 and the varicap diode. C2 set the span of the VCO. The second FET is just an amplifier. **The gain is less than 1, but the current will be higher and the oscillator will not be loaded**.



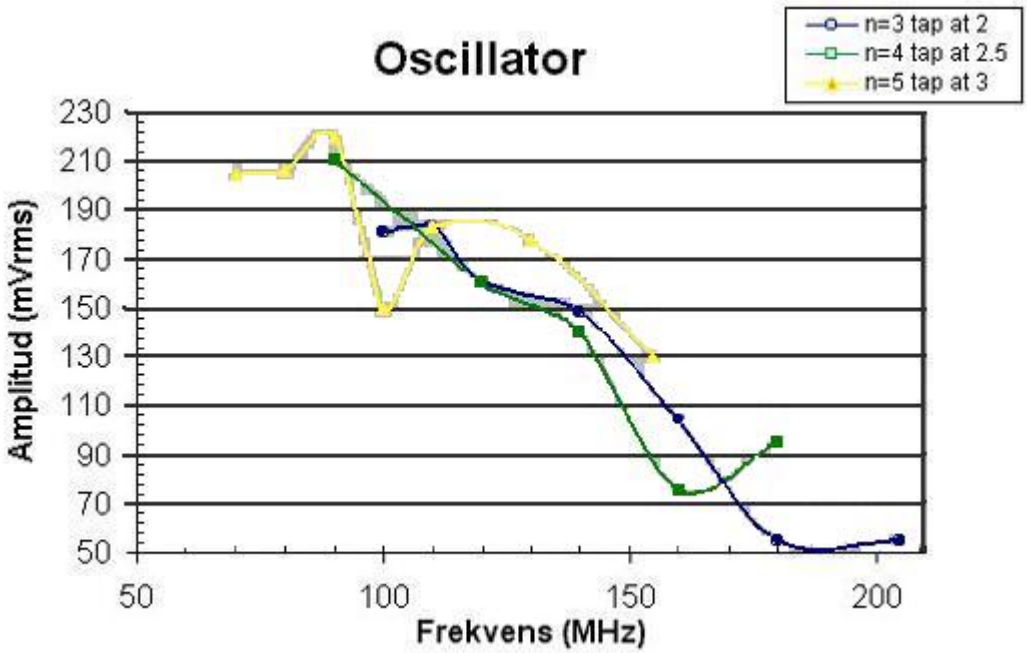
The output amplitude changes depending on the frequency and how many turns there is on L1.

By changing the voltage on g2 at FET1 you can set the amplitude. By adding a resistor to ground you will lower the amplitude.

In this schematic I have connected g2 to Vcc (through R1) which will give the highest gain.

Some data from this VCO

I have made some test with different coils. **The diameter of L1 is the same 7.2mm** but I have changed the turns to 3, 4 and 5. The diagram at the right shows the Amplitude and the frequency. You can also se the range of this VCO.

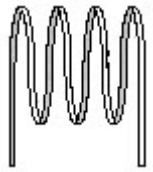


During the test the varicap was removed so the tuning range is set by C1.
The best way to get the oscillator work is to attach a oscilloscope to the output. If the amplitude of the oscillator is low, you must move the tap-point a bit. The best way is to make 3-4 coils with the tap-point at different places and test each coil before you decide which one you will use.
The amplitude from my VCO is about 200mV$_{RMS}$ at 100MHz.

Remember: When you are building oscillators you **must** keep the wires short and shield the oscillator! then it will work nice.

2.2.4 Air Coil Calculation

This side will explain how to calculate coils and will explain how you can make your own coils.
I have made coils with different number of turns and measured the inductance.



Formula :

$$L(uH) = \frac{d^2\ n^2}{18d + 40\ell}$$

$$n = \frac{\sqrt{L(18d+40\ell)}}{d}$$

Where:

- **L** = inductance in microhenrys
- **d** = coil diameter in inches(from wire center to wire center)
- ℓ = coil length in inches (1 inches = 25.4 mm)
- **n** = number of turns

There are lots of Internet-pages explaining how to make coils, but there are few that will give you exact values. I have been experimenting with different diameters, length and wire-diameter and found one good combination. I have been using Hewlett Packard 4192A LF Impedance Analyzer to measure the coils. To make the coils, I have used a two drills with a diameter of 7.2mm and 5.8mm. The diameter is chosen to give wide range of inductance and the coils will get good Q-values. **The wire for the coils has a diameter of 0.6mm. The diameter of the wire is not so critical**. The tables below shows the results.

Number of turns	Inductance (nH) (Compact coil)	Q-value 13-MHz (Compact coil)	Inductance (nH) (Air-space coil)	Q-value 13-MHz (Air-space coil)
3	77	407	66	440
4	122	325	102	560
5	177	340	-	-
6	240	440	206	550
7	306	509	290	690
8	379	607	319	1300
9	470	1500	422	>1500
10	582	>1000	515	>1000
11	644	>1000	-	>1000
12	656	>1000	545	>1000
13	745	>1000	612	>1000
14	789	>1000	658	>1000

INDUCTANCE TABLE (**diameter 5.8 mm**, **0.6mm wire**)				
Number of turns	Inductance (nH) (Compact coil)	Q-value 13-MHz (Compact coil)	Inductance (nH) (Air-space coil)	Q-value 13-MHz (Air-space coil)
4	92	540	79	-
5	131	370	120	530
6	175	340	155	500
7	220	300	184	640
8	272	370	234	560
9	315	470	267	770
10	363	650	313	1270

The coil can be compact with no space between the winding or you can pull it out, to make some space between the windings. My measurements shows that you will get the **best Q-value** if you pull out the winding so the air-space is 0.6mm between the turns in the winding. The inductance will drop a little, se the table above.

- Compact = There is no space between the windings in the coil!
- * Air space= There is an air-space between the winding with the same length as the diameter of the wire you are using (0.6mm in this case).

2.2.5 Air Coils

This side will explain how to make coils with accurate inductance. I have made coils with different number of turns and spacing and measured the inductance with a Wayne Kerr Precision component analyzer 6430A.

Introduction :

How I did the measurement. I used a drill of 7.1mm for all my test coils. Look at figure at right to see the shape of the coil and its end wires.

How to understand the table below:

The first measurement is made when the coil is totally compact (no space between the turns). Then I started to space the end-wires of the coil in 0.1" (2.54mm) step. Lets look at the measurement for 4 turns as an example.

When I made 4 turns the coil was compact and the length between the end wires was almost 0.1". The inductance was 199nH. Then I spaced the coil so the end wires was 0.2" (5.12mm) apart. The inductance was 155nH. Then I spaced the coil so the end wires was 0.3" (7.62mm) apart. The inductance was 128nH...and so on.

Measurement of air coil 7.1mm diam, Wire = 0.5mm Cu			
n=turns	Pad space	Inductance	info
1	0.1 "	60nH	-
2	-	73nH	compact
2	0.1 "	75nH	-
2	0.2 "	72nH	-
3	≈ 0.1 "	150nH	compact
3	0.2 "	112nH	-
3	0.3 "	111nH	-
4	≈ 0.1 "	199nH	compact
4	0.2 "	155nH	-
4	0.3 "	128nH	-
4	0.4 "	127nH	-
5	≈ 0.1 "	275nH	compact
5	0.2 "	205nH	-
5	0.3 "	197nH	-
5	0.4 "	174nH	-
6	≈ 0.15 "	328nH	compact
6	2 "	277nH	-
6	3 "	223nH	-
6	4 "	210nH	-
7	≈ 0.2 "	433nH	compact
7	3 "	311nH	-
7	4 "	289nH	-
7	5 "	242nH	-
8	≈ 0.2 "	508nH	compact
8	3 "	399nH	-
8	4 "	358nH	-
8	5 "	326nH	-
9	≈ 0.2 "	590nH	compact
9	3 "	512nH	-
9	4 "	442nH	-
9	5 "	390nH	-
10	≈ 0.25 "	672nH	compact
10	3 "	603nH	-
10	4 "	514nH	-
10	5 "	461nH	-
10	6 "	409nH	-

2.2.6 Slug Tuned Inductor

This side presents some facts about slug tuned inductors I have been measure the inductance for different winding turns.

Fabr Neosid typ 7x1S
The 7V1S type which I have been testing has a frequency range from 50-200MHz.
The A_L value for this coil is 4,5 nH/n^2
The color of the slug is Green.

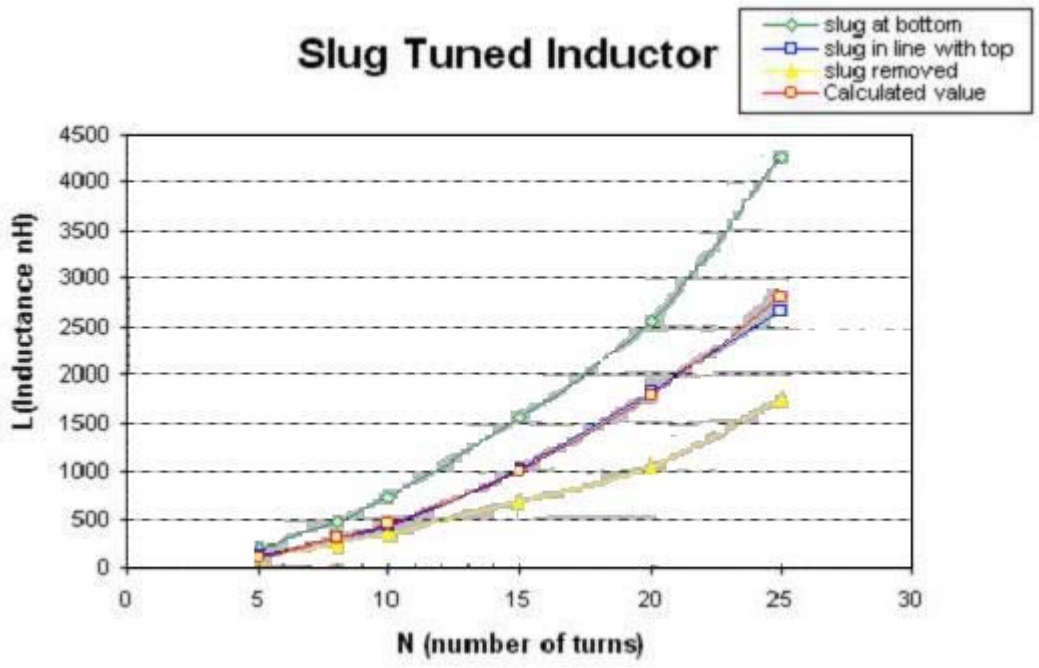
Formula : L (nH) = N^2 *A_L

Where:

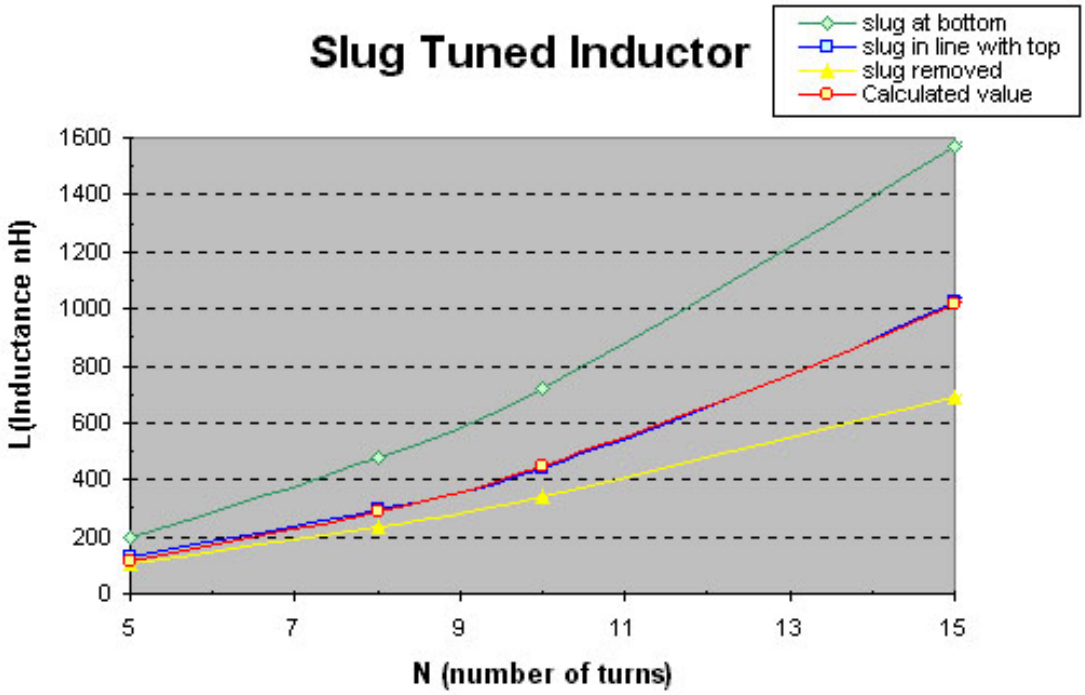
- **L** = inductance in nanohenrys
- **n** = number of turns
- **A_L** = inductance factor

The diagram at the right shows the inductance relative to number of turns.
There is 4 curves:

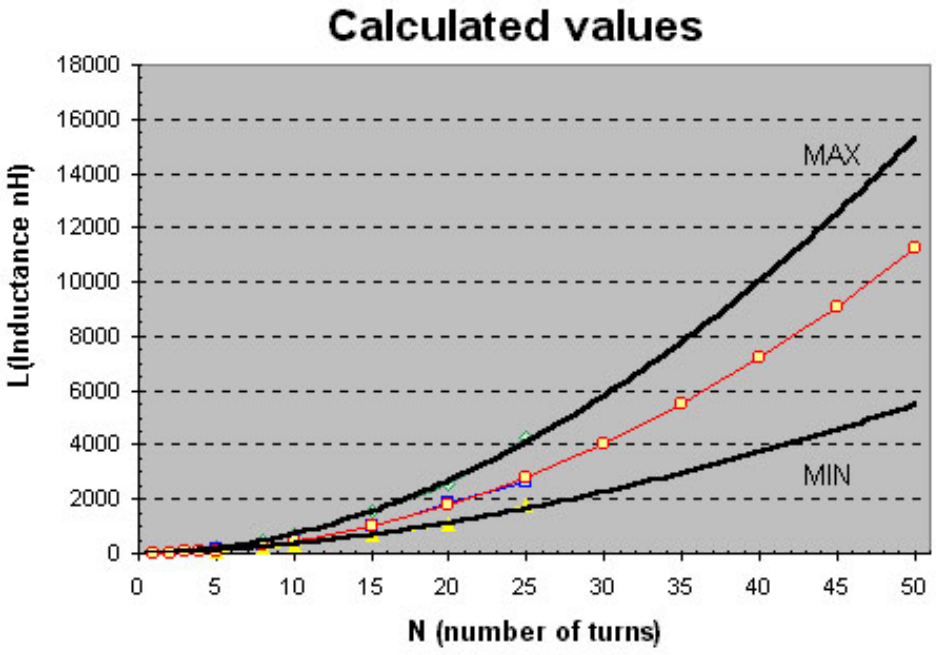
1. The slug is at the bottom of the can.
2. The top of the slug is in line with the top of the can.
3. The slug is totally removed.
4. A theoretically calculated curve.



The diagram at the right is the same diagram as above but has different scale for the lower inductance.



Conclusion: As you can see from the diagram the theoretical value match the blue curve very well.
The area between the Green and the Yellow curve is the span in which you can adjust you inductance value.
The diagram below shows the **calculated** values from MIN, MAX inductance.



Where can I get this can?

You can order this can from ELFA in Sweden article number 58-610-59.

2.2.7 More test about Slug Tuned Inductor

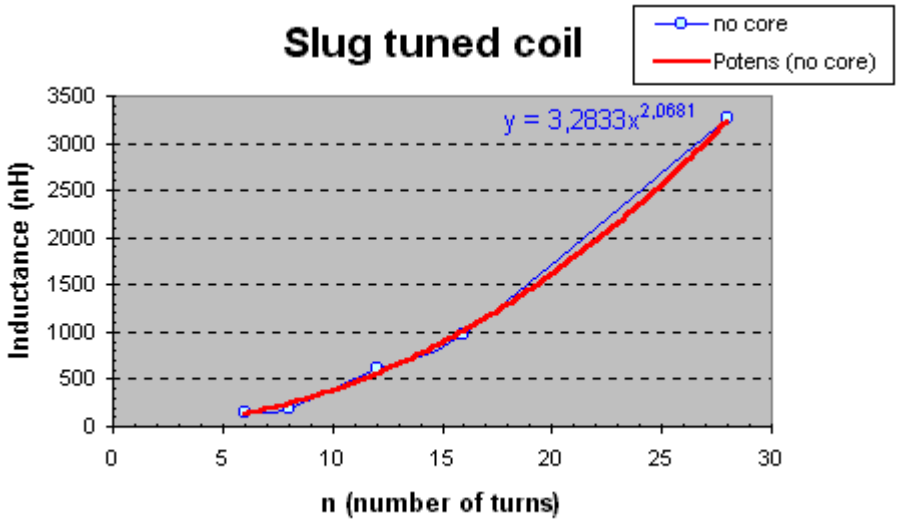
This page investigates some inductor I have got. As always one can never find any info about the coils and there is no manufacture label either so I have to investigate more.

I have made 4 coils with different number of turns. I made 6, 8, 12, ans 28 turns.
There is a formula for coils I will use and I have the been using a LCR meter to measure the inductance of the 4 coils. The values are plotted in excel to form a curve and from the curve I can calculate the $\mathbf{A_L}$ value.
Formula : L (nH) = A_L*n^2

Where:

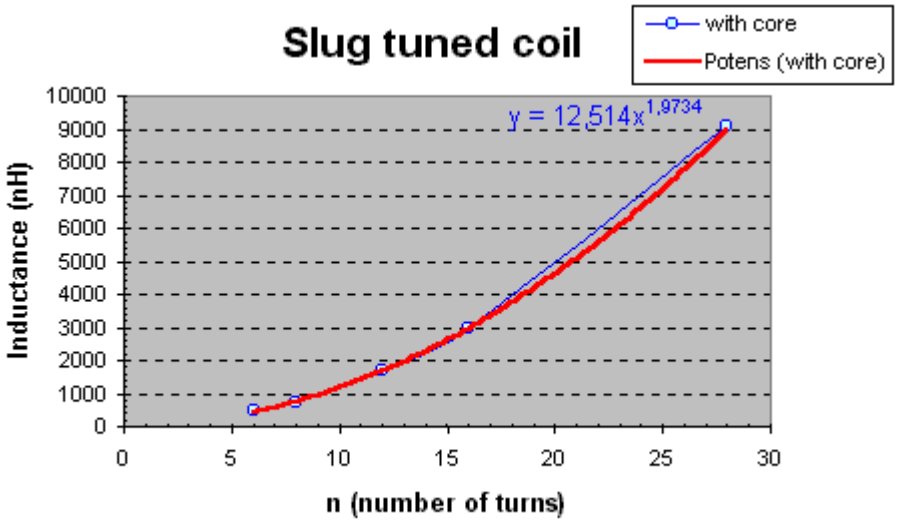
- **L** = inductance in nanohenrys
- $\mathbf{A_L}$ = inductance factor
- **n** = number of turns

This first diagram show the inductance with the screw-slug removed.



The red curve is made by excel and is a trendline. The inductance vary from 150nH to 3263nH.
The formula of the trendline is 3.2833 x $^{2.0681}$
If you compare this formula to he first one you can see the similarity.
The exponent is very close to 2 and the $\mathbf{A_L}$ value will therefore be 3.28

The next diagram show the inductance with the screw-slug screwed to the bottom position.



The red curve is made by excel and is a trendline.
The inductance vary from 457nH to 9113nH.
The formula of the trendline is 12.514 x $^{1.9734}$
The exponent is still very close to 2 and the $\mathbf{A_L}$ value will therefore be 12.51

Conclusion: The ferrite slug core raise the A_L from 3.3 to 12.5, depending on how deep it is screwed into the coil.
The tables below show the complete data. The position of the slug-core is in percent of the total length of the core. If there is no core the value is 0% and if the complete core is screwed into the coil the value is 100%

n = 6	
Core position (%)	Inductance (nH)
0% (no core)	150
16%	170
33%	209
50%	285
67%	372
83%	440
100% (max core)	457

n = 8	
Core position (%)	Inductance (nH)
0% (no core)	198
16%	217
33%	265
50%	341
67%	464
83%	657
100% (max core)	700

n = 12	
Core position (%)	Inductance (nH)
0% (no core)	624
16%	640
33%	690
50%	837
67%	1091
83%	1425
100% (max core)	1701

n = 16	
Core position (%)	Inductance (nH)
0% (no core)	982
16%	1056
33%	1265
50%	1650
67%	2154
83%	2659
100% (max core)	2957

n = 28	
Core position (%)	Inductance (nH)
0% (no core)	3263
16%	3546
33%	4110
50%	5199
67%	6728
83%	8240
100% (max core)	9113

2.3 Circuitos de Amarre de fase.(PLL).(1.2)

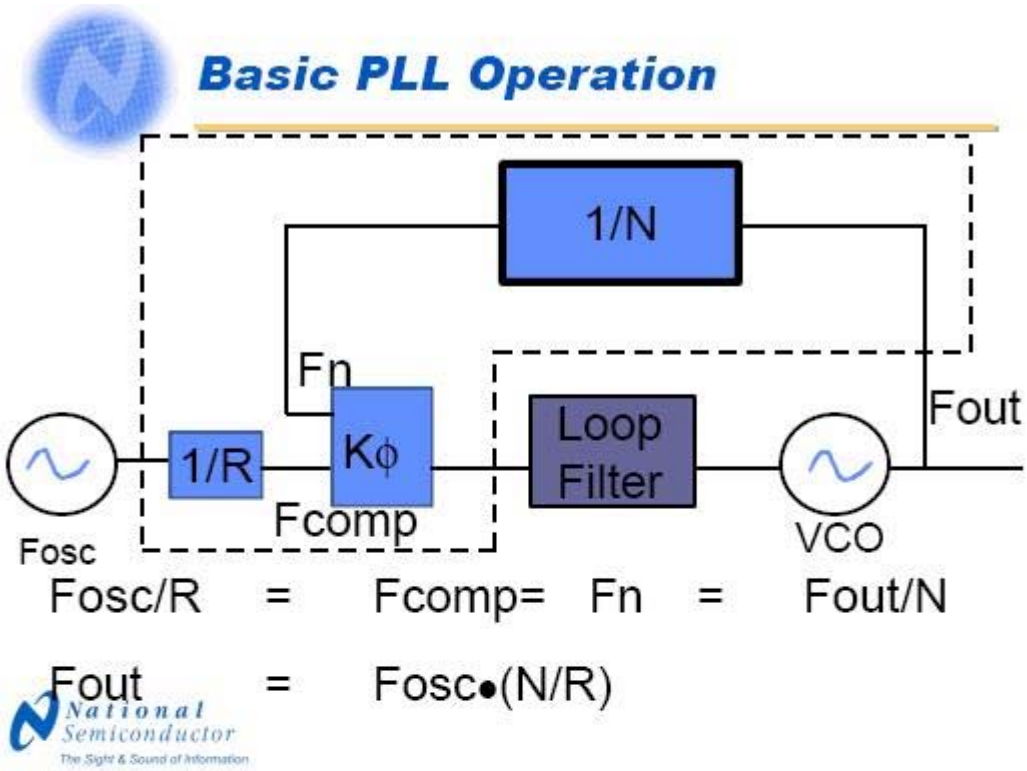
2.3.1 PLL BUILDING BLOCKS.

PRESENTED BY:DEAN BANERJEE.
WIRELESS APPLICATION ENGINEER
National Semiconductors.

Contents.

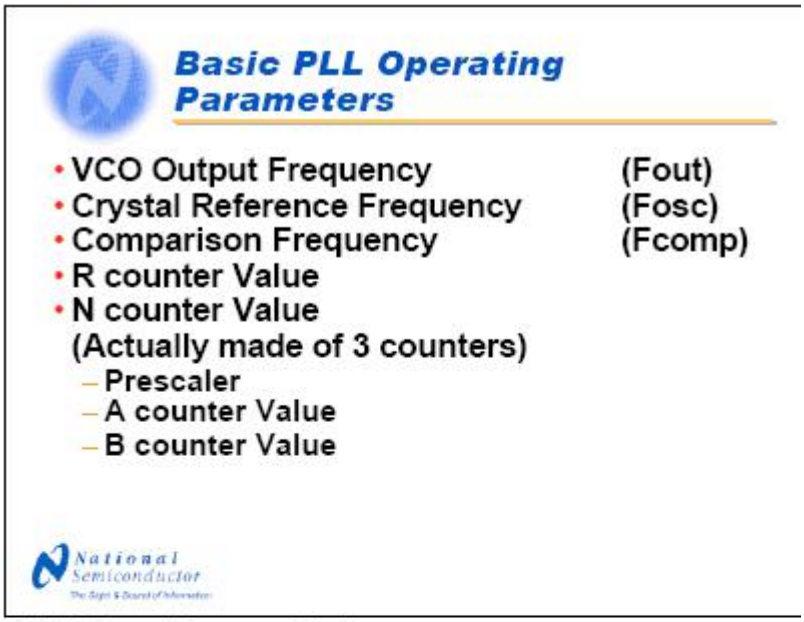
- Basic PLL operation.
- VCO.
- Dividers.
    - R Counter divider.
        - Relation to crystal reference frequency.
        - Relation to comparison frequency.
    - N Counter divider.
        - Prescalers.
        - Legal divide ratios.
    - Programming divider ratios into a PLL.
- Phase frequency detector.
- Charge pump.
- Loop filter.

2.3.1.1 Basic PLL operation.



The way that the PLL works is a follows. There is a fixed crystal frequency (Fosc), which is divided down to the comparison frequency, Fcomp. Now the phase detector compares this signal to Fn. If the signals are the same, it puts out only very small corrections. If Fn>Fcomp, it sinks current. If Fn>Fcomp, it sources current. The loop filter is a low pass filter that converts these current corrections into a voltage. The VCO converts this voltage to a frequency. This output frequency, Fout is divided down by the N counter and compared to Fcomp. So the PLL basically steers the voltage to the VCO such that Fn = Fcomp.

The reason that the VCO can not be simply driven by a DAC is that VCOs have wide process variations and the output frequency can not be accurately determined by the input voltage. Typically, the crystal frequency (Fosc) is very stable, but is limited to much lower frequencies. The PLL also provides the very important advantage that the N counter can be changed by programming it to different values. This allows the PLL to be able to synthesize many different frequencies from a fixed frequency.



VCO Output Frequency (Fout)
This is the output of the whole system, which is controlled by the PLL

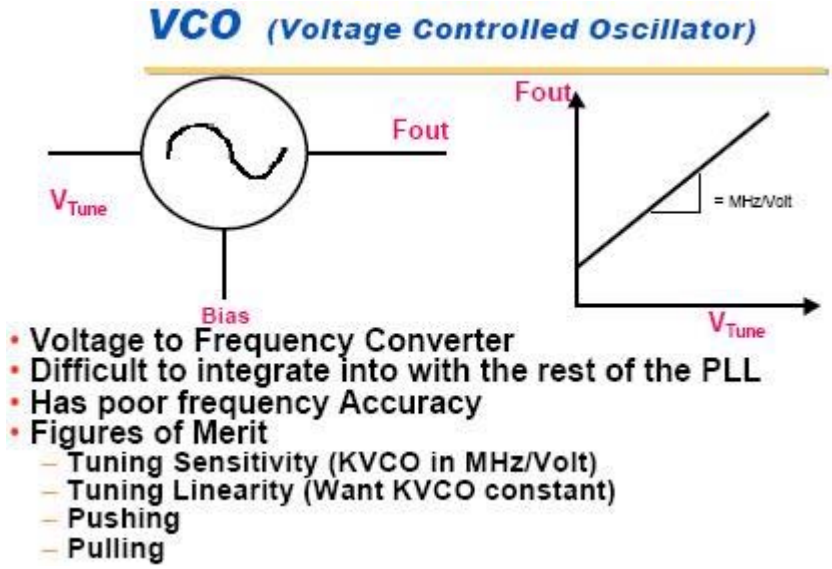
Crystal Reference Frequency (Fosc)
This is a fixed frequency. It can be provided by a TCXO (Temperature Compensated Crystal Oscillator) or a crystal. The crystal oscillator consists of a resonant circuit in the feedback path of an inverter. On some of National's PLLs, an inverter is included for using a crystal. Note that the difference between a crystal and crystal oscillator is that the crystal oscillator includes the inverter.

Comparison Frequency (Fcomp)
This can be thought of as the tuning resolution. As N is changed by 1, the output changes in increments of fcomp. For this reason, it is sometimes referred to as the channel spacing, although that name is not accurate, because there are a few isolated cases where it is something other than the channel spacing (Fractional N).

R Counter Value
This divides the fixed crystal reference frequency by R to get the comparison frequency. R is usually fixed for a given application.

N Counter Value
This multiplies the comparison frequency in order to get the output frequency. Note that the output frequency is tuned by changing the N counter value. The N counter actually consists of smaller counters in order to allow high frequency operation.

2.3.1.2 VCO



VCO terminology.

Tuning sensitivity, Modulation sensitivity, or KVCO.
This is how much the output frequency changes for a given change in the voltage.

Tuning linearity.
Although design equations assume that the VCO gain is linear within some range, it typically has some non linear characteristics.
Usually the tuning sensitivity is less at the higher tuning voltages.

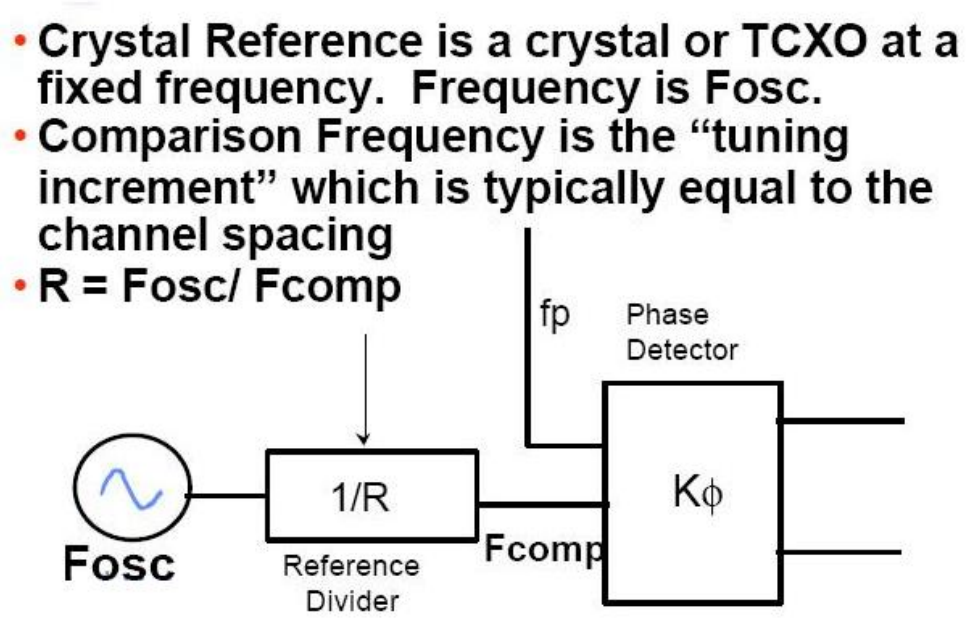
Pulling.
This the drift in the output frequency caused by loading the VCO.

Load pushing.
A drift in the output frequency caused by changing the power supply voltage. One way to express this is in Mhz/volt. It also gives an indication of how vulnerable the VCO is to power supply noise.

Other comments.
The VCO contributes noise to the system. This is mostly outside the loop bandwidth

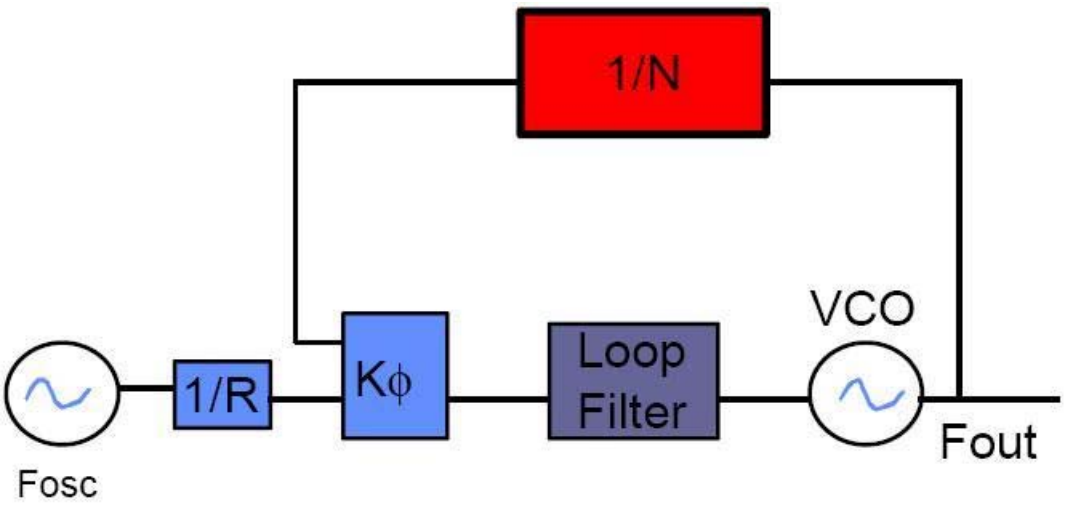
2.3.1.3 Dividers

contiene desde texto 6 hasta texto 14



To determine what value should be programmed into the R counter, the comparison frequency must be known first. The comparison frequency is often chosen equal to the channel spacing since when N is changed by 1, the output frequency is changed by 1*Fcomp. Choosing the comparison frequency larger than this would cause the PLL to skip over channels, so this can not be done. The comparison frequency could be chosen smaller, but this would result in worse phase noise and a slower lock time -- the performance would not be as good. The restriction that the comparison frequency can not be chosen larger than the channel spacing applies only to integer N PLLs, not fractional N PLLs.

The crystal reference must be chosen so that is an integer multiple of the comparison frequency. Since Fcomp = Fosc / R, the value from the R counter can be easily determined.



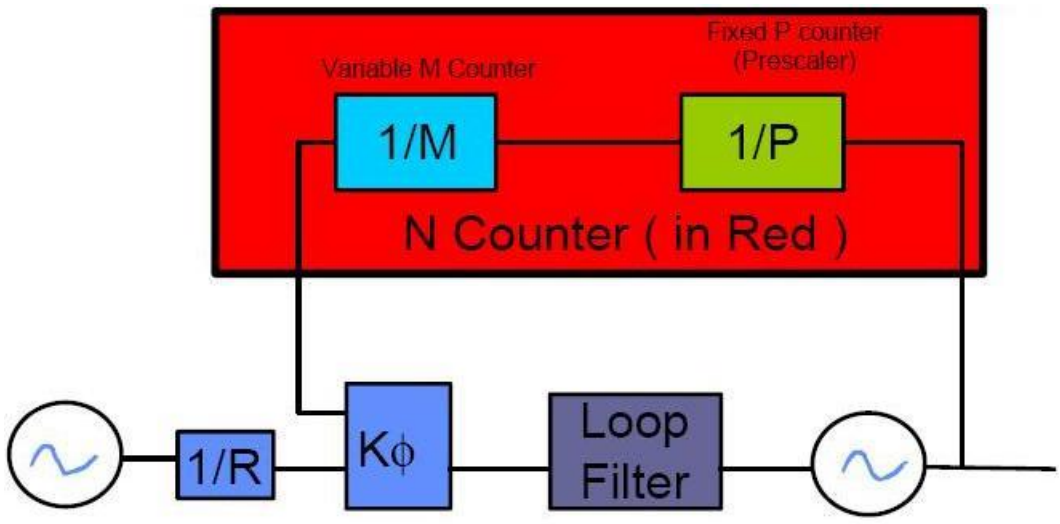
Problem **High frequency Output makes this not practical for CMOS**

N Value Calculation

N is simply the output frequency divided by the comparison frequency.

Problem with Using a Simple Counter for the N Counter

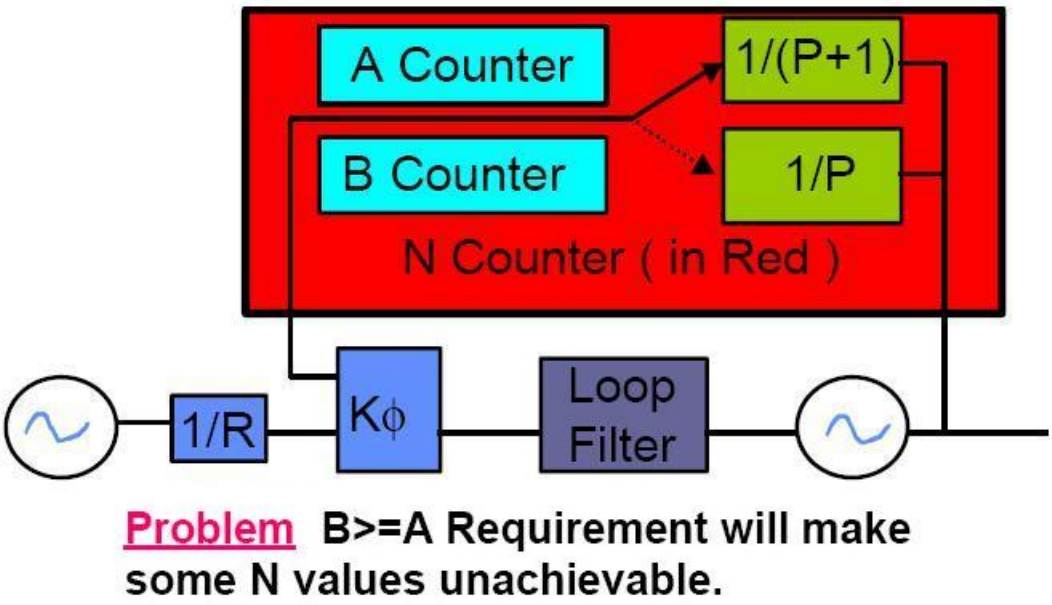
However, since the output frequency is typically high frequency, it is not practical to build it as a single counter because the high frequency process is good for the high frequency signal, but not so good for the rest of the functions on the PLL. This is why this is not used, except for low frequency.



Problem Frequency Resolution is decreased

Single modulus Prescaler.
This gets around the high frequency problem but sacrifices tuning resolution.
This why the dual modulus Prescaler (next slide) is typically used.

It is possible to reduce the comparison frequency by a factor of P, but this results in a higher noise and higher reference spurs.



Dual Modulus Prescaler operation.

1. Initially the size P+1 prescaler is used.
2. Every P+1 cycles of the VCO, both the A and the B counters are decreased by 1.
3. This is continued until A=0. this takes a total of A * (P+1) VCO cycles.
4. Now the size P prescaler is switched in. Every P VCO cycles, the counter B is decreased by 1 since the B counter was previously counting this takes (B-A)* P VCO cycles
5. When the B counter reaches 0, 1 pulse is given to the fp signal. This result in making N=A*(P+1) + (B-A)*P = P*B + A. Note also that this implies B >=A for proper operation.

Dual Modulus Prescaler Operation

- In the previous slide, the size P+1 prescaler is first used, until the A counter reaches 0
  - This takes a total of A•(P + 1) counts
  - The B counter is simultaneously counting down
- The size P Prescaler is then switched in
  - The B counter starts with (B - A) counts
  - This takes (B - A)•P counts. This implies for proper operation that B>=A
- Adding the total counts gives the relationships
  - N = P•B + A
  - B = N div P, A = N mod P

Determining The N Counter Value

- P = Prescaler setting
- N = Fosc / Fcomp
- A requirement for proper operation of the PLL is B>=A
  - B = N div P
  - A = N - (B • P) = N mod P (Note A < P)
  - N = A(P+1) + (B-A)P = PB + A
  - Minimum Continuous Divide Ratio
    - If N >= P •(P-1) this guarantees B>=A
    - This does not mean N>=P •(P+1) is a necessary condition.
  - Note that B and A are programmed directly in the N register

To program in a value for the N counter, the A counter, B counter, and prescalers are specified, which specifies N. Note from the proceeding slide that B>=A. This must be checked for each value of N programmed into the chip. A prescaler must be chosen before these calculations are used. e.g. for a 64/65 prescaler, P = 64

Recall:

equation 1: $N = P*B + A$

to determine B, apply the div operation (also called "trunc" which means divide and disregard the remainder) to both sides of the equation to yield:

$N \text{ div } P = (P*B + A) \text{ div } P = P*B \text{ div } P + A \text{ div } P = B$

(recall that $A \text{ div } P = 0$ since $A < P$)

$\mathbf{B = N \text{ div } P}$

Once B is known, A can be determined algebraically, or by applying the mod operation (short for "modulo", which means disregard the quotient and take only the remainder)

$N \bmod P = (P*B+A) \bmod P = P*B \bmod P + A \bmod P = A \bmod P$

$\mathbf{A = N \bmod P}$

The minimum continuous divide ratio is a sufficient condition, but not a necessary condition. In other words, there are a few isolated cases where $N < P*(P-1)$, yet the prescaler is still usable.

If **N>= P*(P-1)**, then **B>=P-1**. However, since A<P, this guarantees **B>=A**. This is convenient in checking a range of N values.

Dual Modulus Prescaler Example

- Assume the Following:
  - Fout = 1000 MHz
  - Fosc = 10 MHz
  - Fcomp (channel spacing) = 100 KHz
  - P = 128
- Determine Counter Values
  - R = Fosc / Fcomp = 10 MHz / 100 KHz = 100
  - N = Fout / Fcomp = 1000 MHz / 100 KHz = 10000
  - B = N div P = 10000 div 128 = TRUNC(78.13) = 78
  - A = N - (B • P) = 10000 mod 128 = 16

Note that is is first necessary to select a prescaler to use. In this case, a 128/129 prescaler is used. If the initial selection of prescaler does not work, they try a different prescaler. The available prescalers are specified in the selection guide and the data book. After the prescaler is chosen, it is essential to confirm that B>= A for that particular value of N for proper operation.

For this particular example, the minimum continuous divide ratio is 128*(128-1) = 16256. Since 16256 is greater than N = 10000, we can not conclude yet that this is a legal N value, and it is necessary to check B>=A. Had N been greater than 16256, the work would have been done. Here is a summary of some of the other N values.

N	B	A	Legal Divide Ratio?
10000	78	16	yes
10001	78	17	yes
. . .			
10062	78	78	yes
10063	78	79	no
. . .			
10111	78	127	no
10112	79	0	yes

Sufficient Prescaler Conditions

(If these conditions are met, then the necessary conditions will also be met. Note that this assumes an 11 bit B counter.)

Prescaler	Min. N (Continuous)	Max. N
8/3	56	16383
16/17	240	32767
32/33	992	65535
64/65	4032	131071
128/129	16256	262143
P/(P+1)	P•(P-1)	2047•P+P-1

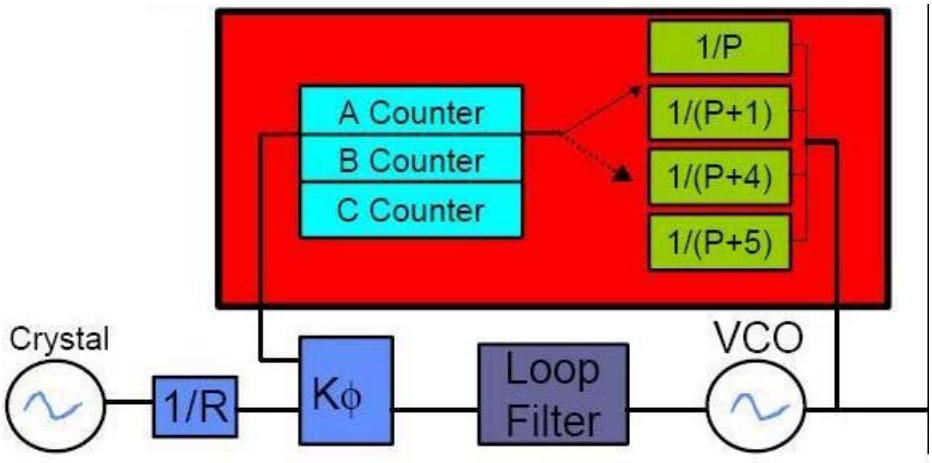
This chart is included for reference.

The minimum N value is the minimum continuous divide ratio for the given prescaler. Note that smaller prescalers have lower minimum continuous divide ratios.

The maximum value of N is limited by the fact that the B counter has a finite number of bits. In this case, it is assumed that the B counter has 11 bits. This is true of the majority of National's PLLs.

This chart can be used to help determine which prescaler can be used. If the desired value of N is below the minimum N listed, it still may be achievable, and the only way to know is to check B>=A. Note that this assumes an 11-Bit B counter. Some parts have a different size B counter.

Also be aware that for the lmx2350/52 only, these parts have the requirement B>=A+2. This rule only applies to these 2 parts.



- **Advantage** Allows lower divide ratios.
- N = P•C + 4•B + A

Quadruple Modulus Prescaler Operation

The quadruple modulus prescaler works by having four possible values to use as a prescaler, although only three are used for any given N value.

Solving for C, B, and A

A greatly simplifying assumption is that P is a multiple of 4. Practically, this turns out to be true just about all the time. Assuming this, we get:

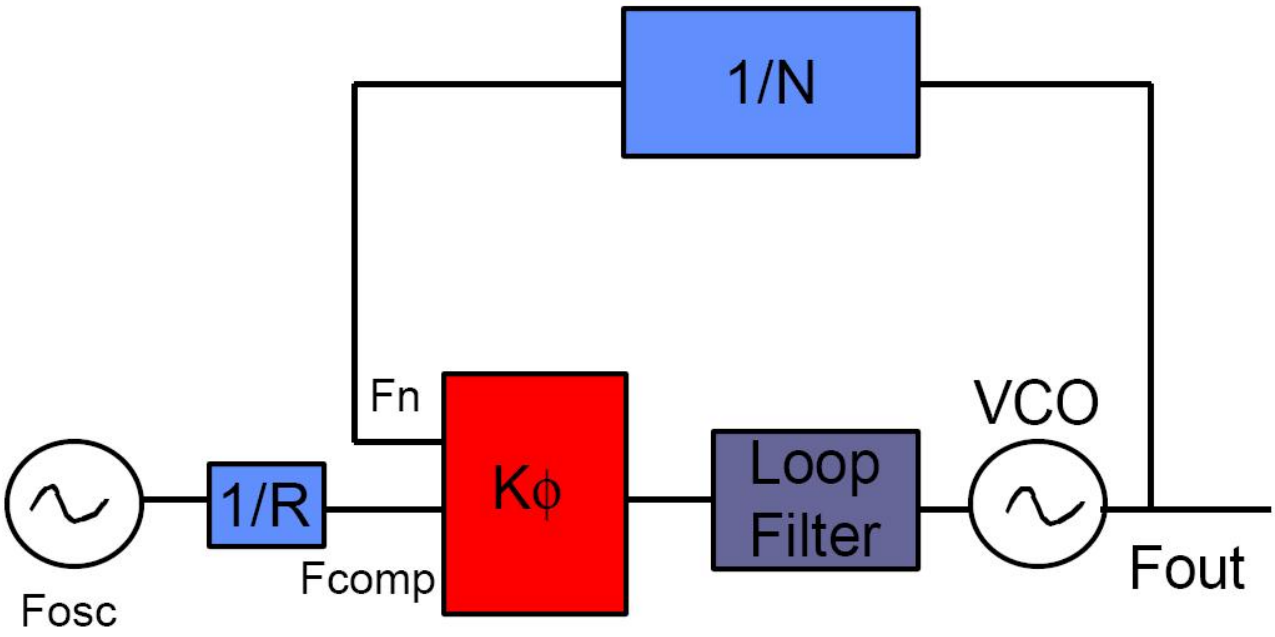
$C = N \text{ div } P$

$A = N \bmod 4$

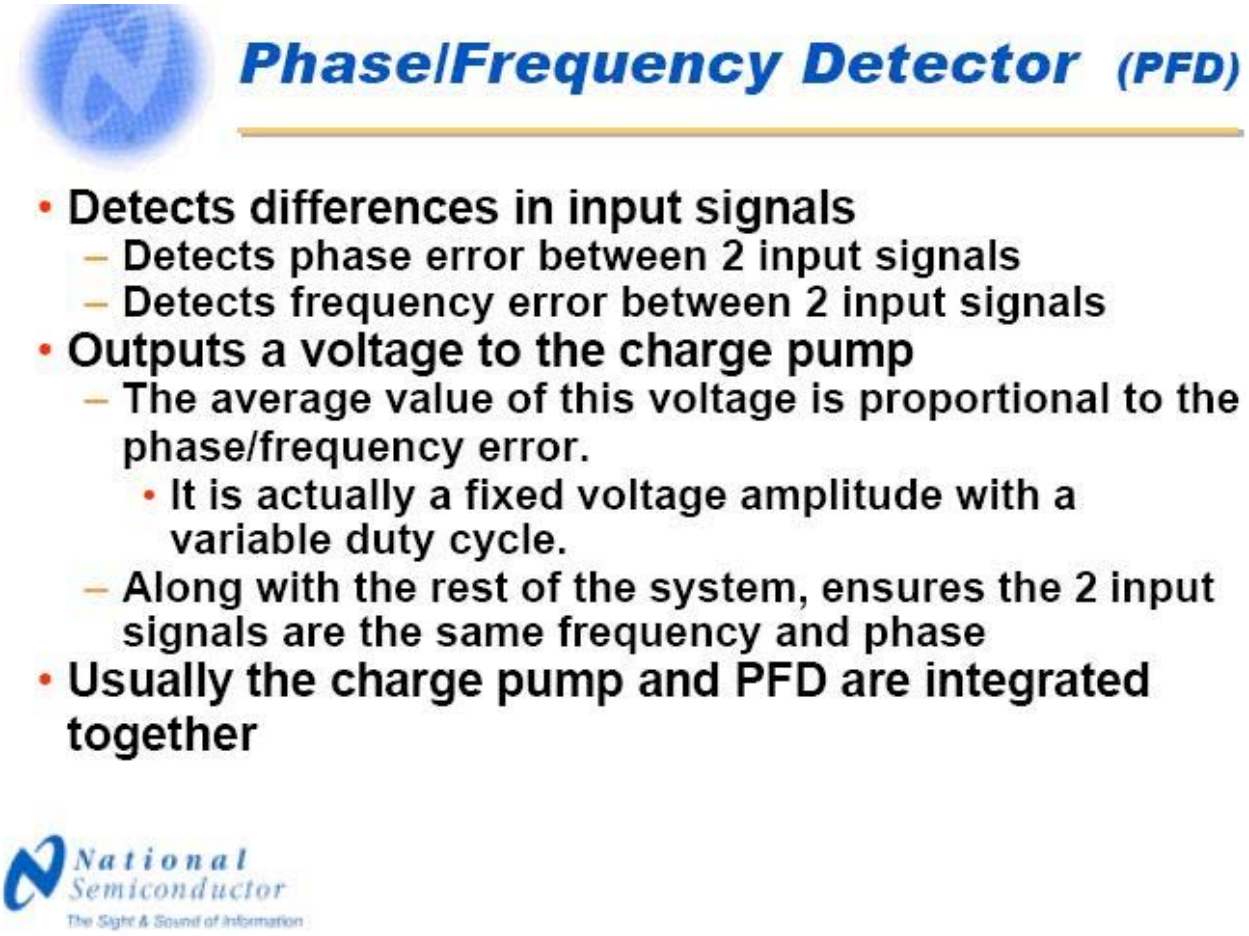
$B = (N - P*C)/4$

Note that $C >= \max\{A,B\}$ for proper operation

Note that $A < 4$ and $B < P/4$ are restrictions for A and B as well.

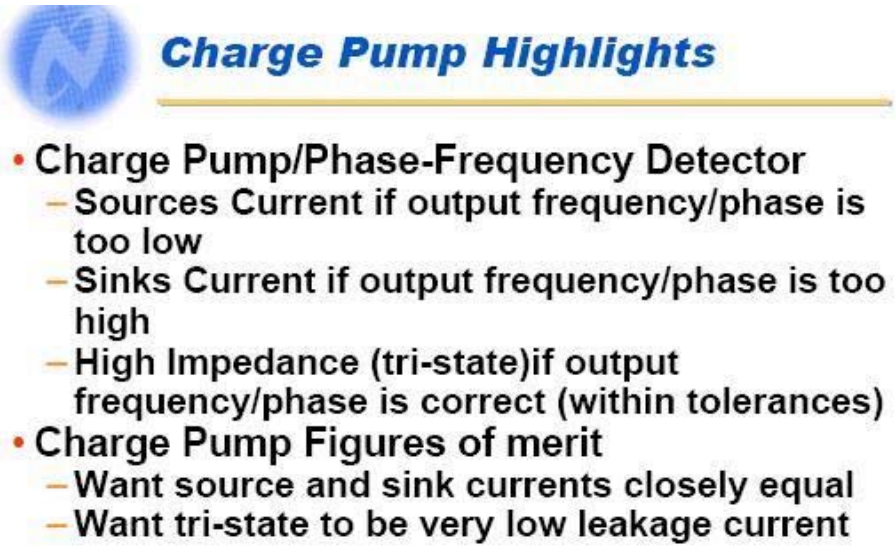


2.3.1.4 Phase frequency detector.



The phase - frequency detector is integrated with the charge pump. On some PLLs, the outputs ϕr and ϕp are given so that an external charge pump can be used.

2.3.1.5 Charge pump.

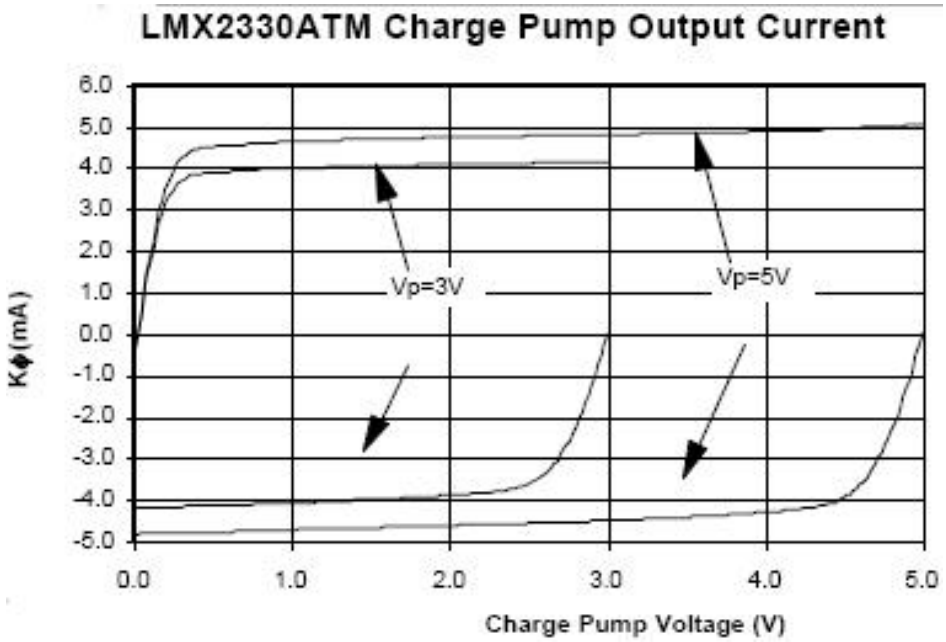


In the PLL, the comparison frequency is compared with the frequency obtained by dividing Fout/N, often denoted fp. If these 2 frequencies are the same, then the PLL is considered to be in lock and theoretically, the output of the charge pump should be 0 (high impedance state). In practice there are alternating positive and negative pulses of current with a period equal to the reference period, and these pulses are about 20-50 nS wide.

When out of lock, either positive or negative pulses are given to adjust the voltage on the loop filter, which adjusts the output frequency. For instance, when the output frequency is too low, there are positive pulses pulses of current, the width of these pulses increases with the amount that the PLL is out of lock, which increase the VCO voltage, which increase the output frequency.

Theoretically, the charge pump should sink and source the same amount of current, but in practice, there will always be some degree of mismatch. This mismatch can cause reference spurs and effect lock time, and is undesirable.

National specifies a typical and maximum mismatch in the databook. The charge pump current can also vary with the voltage on the loop filter, and over temperature.



The charge pump has 3 states:

1. Sink Current
2. Source Current
3. Tri-state (High Impedance)

This slide shows that the amount of current sunk and sourced changes with the supply voltage and with the charge pump voltage (which is equal to the tuning voltage to the VCO). Inferences about charge pump mismatch and variation can be made from this slide. Typically, the charge pump is not operated " Near the Rails", since the graph looks very nonlinear in this region. Note that these curves are inverted. The reason for the inversion is the way that National tests charge pump currents.

Charge Pump Mismatch

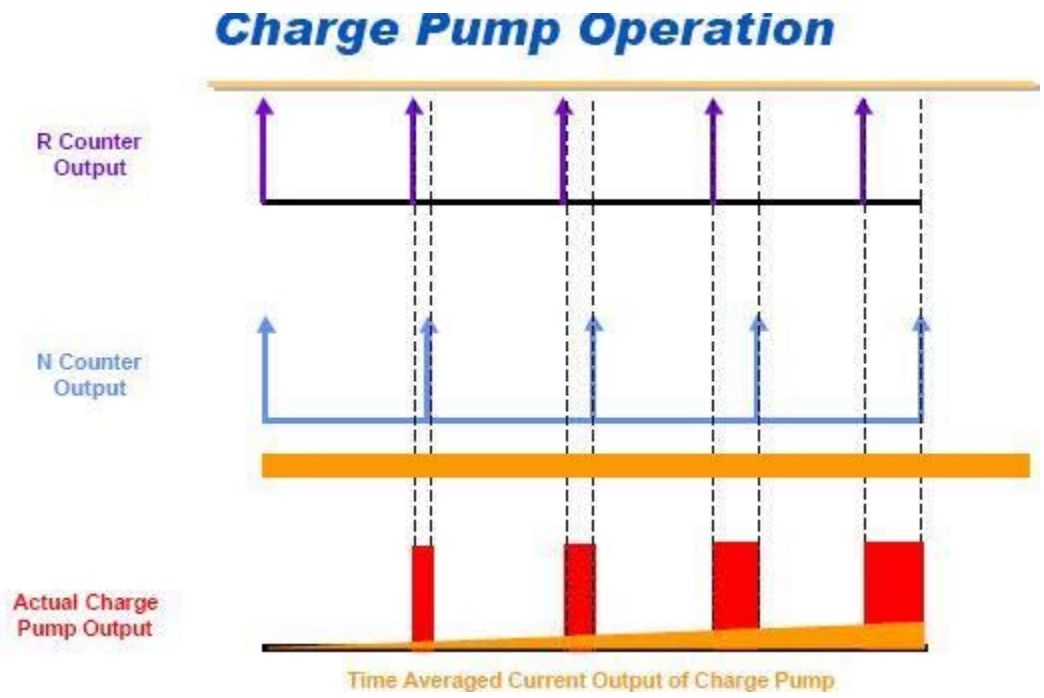
Charge pump mismatch is a measure of how well the sink and the source currents are matched. 0% mismatch is theoretically the most desirable, but sometimes a slight positive mismatch is desirable because the turn on time of the source transistor is slower than the turn on time of the sink transistor.

Charge Pump Balance

Balance describes how constant the charge pump currents over the charge pump voltage. A perfectly balanced charge pump would put out the exact same amount of current regardless of the charge pump voltage.

Charge Pump Leakage

Actually, the graph on this slide has nothing to do with charge pump leakage, although this is also an important parameter. In the locked state, the charge pump is off for most of the time. When the charge pump is off, the current should be 0 mA, but in fact there is a very slight current (usually in the nA range) when the charge pump current is off.



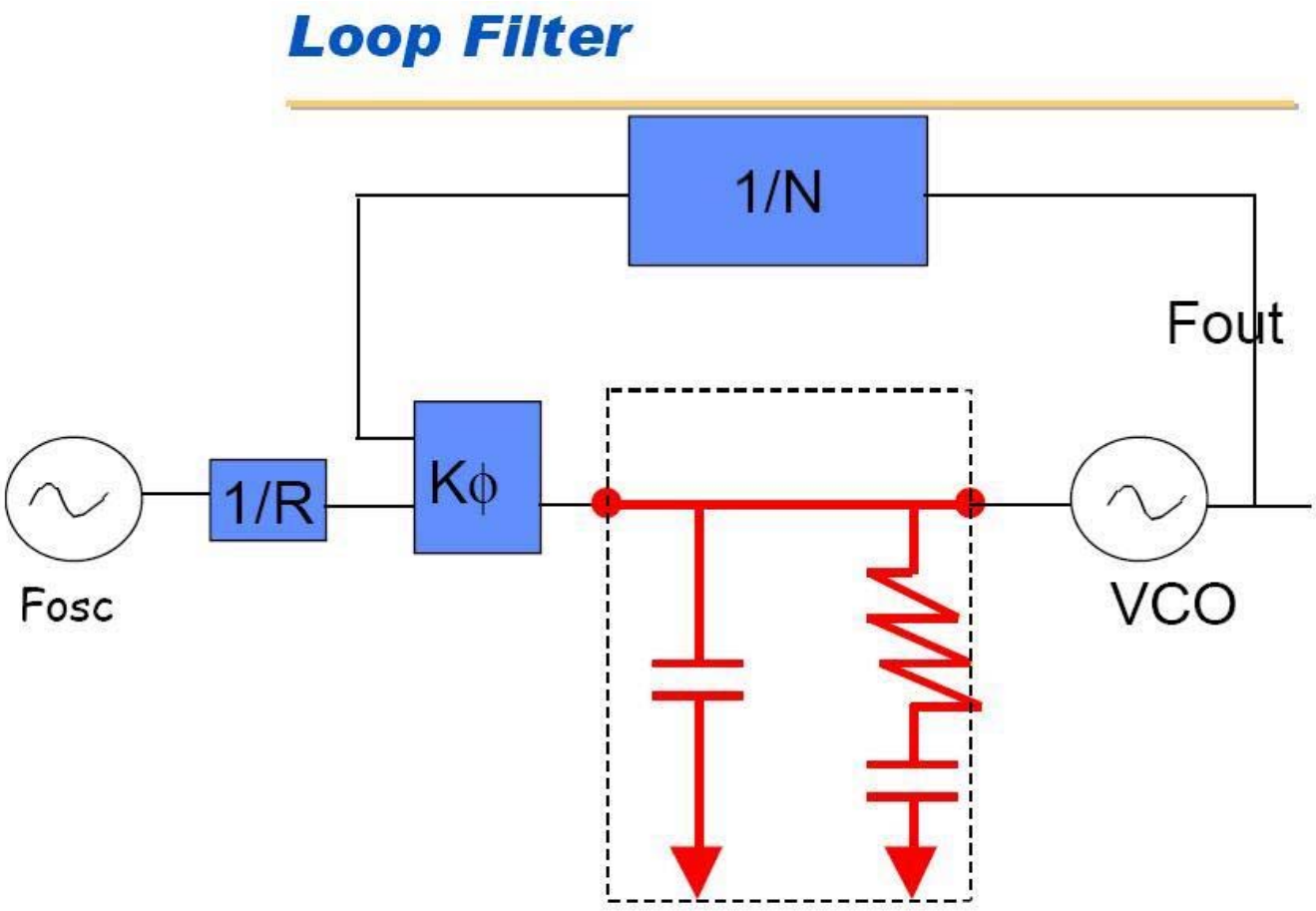
Charge Pump Operation

The charge pump puts out a pulse width modulated signal. It can source current, sink current, or be high impedance. Whenever the R counter has a positive transition, there is a positive transition for the charge pump output. That means if it was sinking current, it is tri-state. If it was tri-state, it sources current. If it was already sourcing current, it continues to source current. Whenever the N divider has a positive transition, the charge pump has a negative transition. This means that if the charge pump was sourcing current, it becomes tri-state. If it was tri-state, it sinks current. If it was already sinking current, it continues to sink current.

Continuous Time Approximation

For the sake of simplicity, it is usually fair to model the charge pump current as an analog current which has a value equal to the time-averaged value. This value is shown with the orange curve. This approximation is the continuous time approximation and is valid provided that the sample rate is sufficiently high relative to the bandwidth of the loop filter. The loop bandwidth will be discussed in later sections.

2.3.1.6 Loop filter.

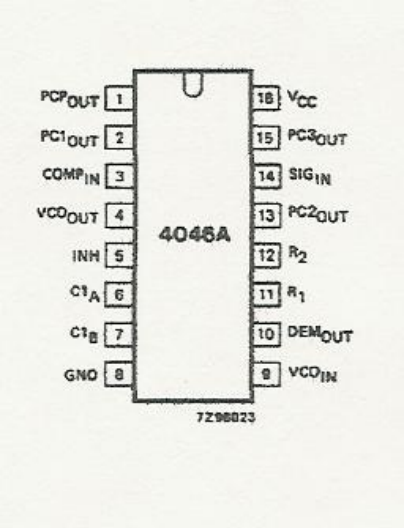


Loop Filter

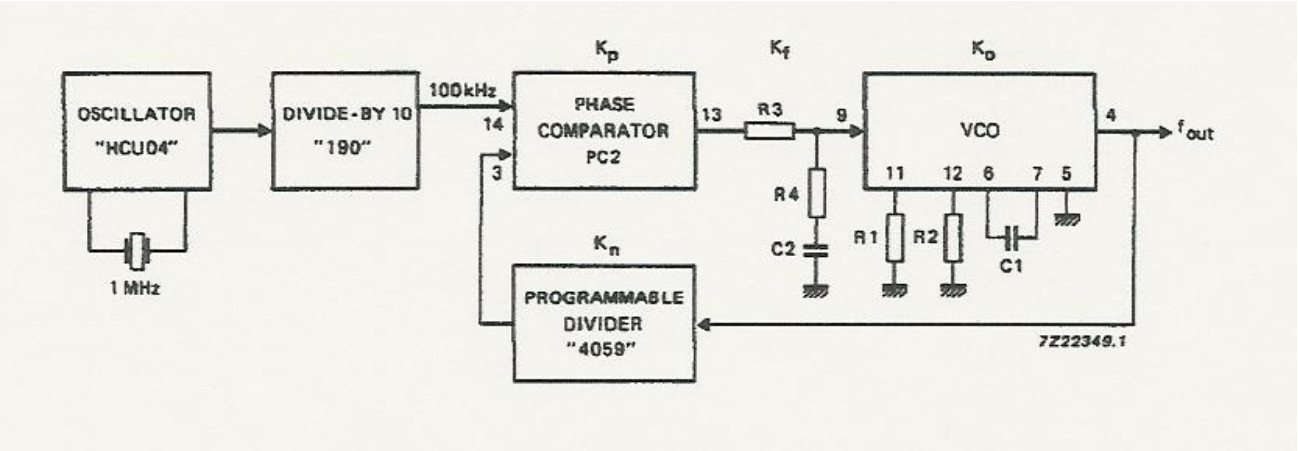
- The Loop Filter is a Low Pass Filter
  - It can also be thought of as an integrator with some added components
- The Loop Filter determines a lot about PLL performance
  - Switching Time
  - Loop Bandwidth (Related to RMS Error)
  - Reference Spurs
- The Loop Filter is external to the chip and is application specific
  - National Has Loop Filter Design Software at wireless.national.com (EasyPLL)

2.3.2 74HC4046 phase-locked-loop

The 74HC4046 phase-locked-loop which is an integrated circuit contains a voltage controlled oscillator and will work as high as 17 Mhz.
With the 74HC4046 VCO, its tuning range is determined by one external capacitor C1 (between C1A and C1B) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. Look at the 74HC4046 page.



4046A pinout



Frequency sinthesizer

2.3.3 MAX2622/MAX2623/MAX2624

General Description

The MAX2622/MAX2623/MAX2624 self-contained voltage controlled oscillators (VCOs) combine an integrated oscillator and output buffer in a miniature 8-pin µMAX package. The inductor and varactor elements of the tank circuits are integrated on-chip, greatly simplifying application of the part. In addition, the center frequency of oscillation and frequency span are factory preset to provide a guaranteed frequency range versus control voltage. An external tuning voltage controls the oscillation frequency. The output signals are buffered by an amplifier stage matched on-chip to 50Ω.

The MAX2622/MAX2623/MAX2624 operate from a +2.7V to +5.5V supply voltage and require only 8mA of supply current. In shutdown mode, the supply current is reduced to 0.1µA.

Applications

866MHz to 868MHz European ISM Band (MAX2622)
DECT 1/2 Frequency LO (MAX2623)
902MHz to 928MHz ISM Band, ±10.7MHz IF (MAX2623)
902MHz to 928MHz ISM Band, 45MHz to 70MHz IF (MAX2624)

Features

_ Fully Monolithic
_ Guaranteed Performance
_ On-Chip 50Ω Output Match
_ Wide Choice of Frequencies
855MHz to 881MHz (MAX2622)
885MHz to 950MHz (MAX2623)
947MHz to 998MHz (MAX2624)
_ +2.7V to +5.5V Single-Supply Operation
_ Low-Current Shutdown Mode
_ Smaller than Modules (8-Pin µMAX Package)

2.3.4 NBC12430

3.3 V/5 V_Programmable
PLL Synthesized Clock
Generator
50 MHz to 800 MHz

The NBC12430 is a general purpose, PLL based synthesized clock source. The VCO will operate over a frequency range of 400 MHz to 800 MHz. The VCO frequency is sent to the N-output divider, where it can be configured to provide division ratios of 1, 2, 4, or 8. The VCO and output frequency can be programmed using the parallel or serial interfaces to the configuration logic. Output frequency steps of 250 KHz, 500 KHz, 1.0 MHz, 2.0 MHz can be achieved using a 16 MHz crystal, depending on the output dividers settings. The PLL loop filter is fully integrated and does not require any external components.

- Best-in-Class Output Jitter Performance, ±20 ps Peak-to-Peak
- 50 MHz to 800 MHz Programmable Differential PECL Outputs
- Fully Integrated Phase-Lock-Loop with Internal Loop Filter
- Parallel Interface for Programming Counter and Output Dividers During Power-Up
- Minimal Frequency Overshoot
- Serial 3-Wire Programming Interface
- Crystal Oscillator Interface
- Operating Range: VCC = 3.135 V to 5.25 V
- CMOS and TTL Compatible Control Inputs
- Pin Compatible with Motorola MC12430

2.4 Modulador de ancho de pulso.(1.3)

2.4.1 Pulse Width Modulation (PWM) Basics

There are many forms of modulation used for communicating information. When a high frequency signal has an amplitude varied in response to a lower frequency signal we have AM (amplitude modulation). When the signal frequency is varied in response to the modulating signal we have FM (frequency modulation. These signals are used for radio modulation because the high frequency carrier signal is needs for efficient radiation of the signal. When communication by pulses was introduced, the amplitude, frequency and pulse width become possible modulation options. In many power electronic converters where the output voltage can be one of two values the only option is modulation of average conduction time.

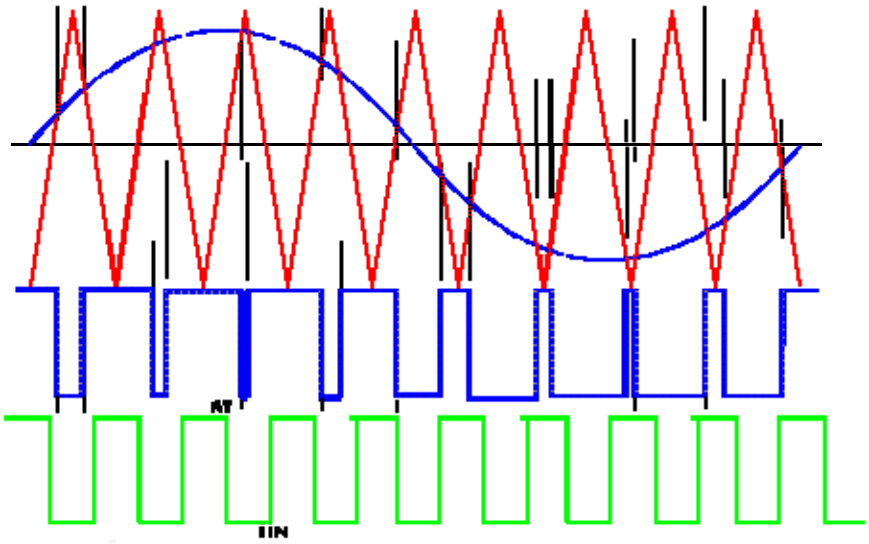


Fig. 1: Unmodulated, sine modulated pulses

2.4.1.1 1. Linear Modulation

The simplest modulation to interpret is where the average ON time of the pulses varies proportionally with the modulating signal. The advantage of linear processing for this application lies in the ease of de-modulation. The modulating signal can be recovered from the PWM by low pass filtering. For a single low frequency sine wave as modulating signal modulating the width of a fixed frequency (fs) pulse train the spectra is as shown in Fig 2. Clearly a low pass filter can extract the modulating component fm.

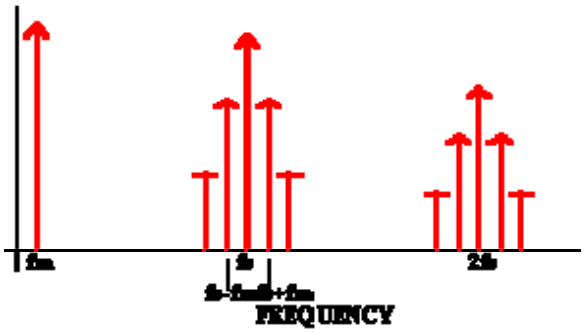


Fig. 2: Spectra of PWM

2.4.1.2 2. Sawtooth PWM

The simplest analog form of generating fixed frequency PWM is by comparison with a linear slope waveform such as a sawtooth. As seen in Fig 2 the output signal goes high when the sine wave is higher than the sawtooth. This is implemented using a comparator whose output voltage goes to a logic HIGH when no input is greater than the other.

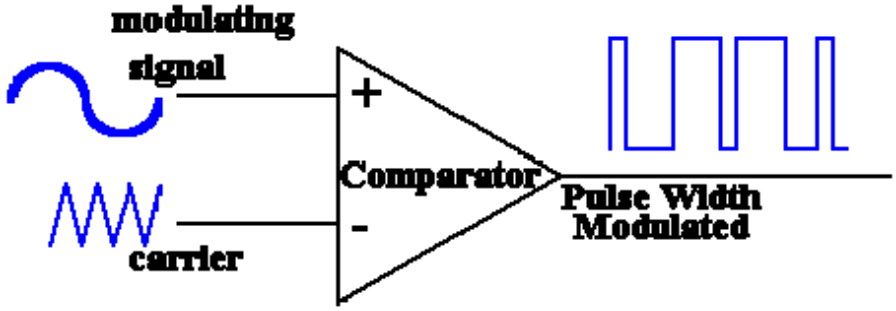


Fig. 3: Sine Sawtooth PWM

Other signals with straight edges can be used for modulation a rising ramp carrier will generate PWM with Trailing Edge Modulation.

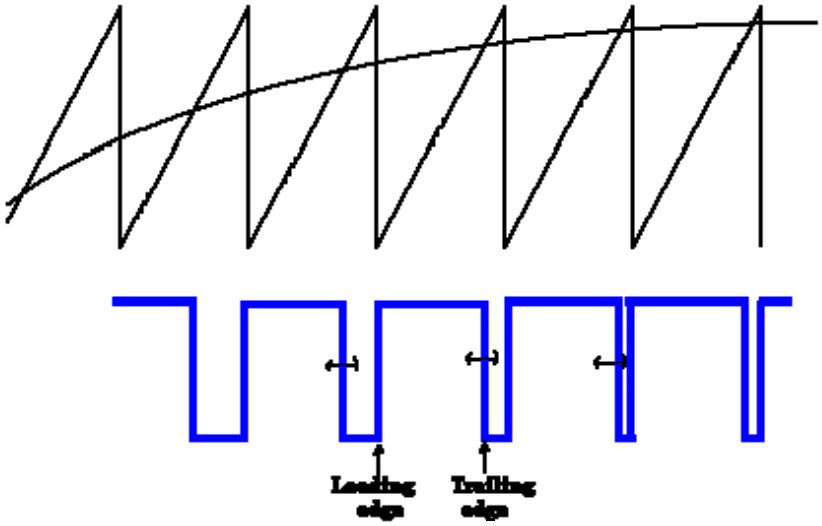


Fig. 4: Trailing Edge Modulation

It is easier to have an integrator with a reset to generate the ramp in Fig 4 but the modulation is inferior to double edge modulation.

2.4.1.3 3. Regular Sampled PWM

The scheme illustrated above generates a switching edge at the instant of crossing of the sine wave and the triangle. This is an easy scheme to implement using analogue electronics but suffers the imprecision and drift of all analogue computation as well as having difficulties of generating multiple edges when the signal has even a small added noise. Many modulators are now implemented digitally but there is difficulty is computing the precise intercept of the modulating wave and the carrier. Regular sampled PWM makes the width of the pulse proportional to the value of the modulating signal at the beginning of the carrier period. In Fig 5 the intercept of the sample values with the triangle determine the edges of the Pulses. For a sawtooth wave of frequency fs the samples are at 2fs.

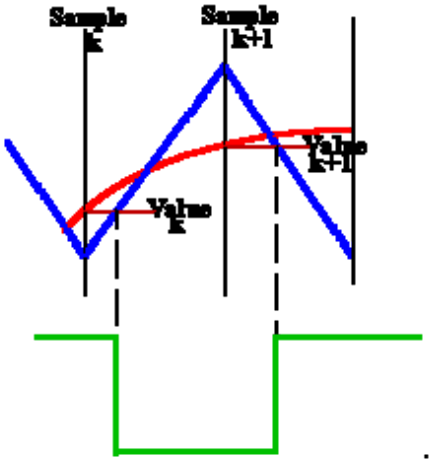


Fig. 5: Regular Sampled PWM

There are many ways to generate a Pulse Width Modulated signal other than fixed frequency sine sawtooth. For three phase systems the modulation of a Voltage Source Inverter can generate a PWM signal for each phase leg by comparison of the desired output voltage waveform for each phase with the same sawtooth. One alternative which is easier to implement in a computer and gives a larger MODULATION DEPTH is using SPACE VECTOR MODULATION.

2.4.1.4 4. Modulation Depth

For a single phase inverter modulated by a sine-sawtooth comparison, if we compare a sine wave of magnitude from -2 to +2 with a triangle from -1 to +1 the linear relation between the input signal and the average output signal will be lost. Once the sine wave reaches the peak of the triangle the pulses will be of maximum width and the modulation will then saturate. The **Modulation depth** is the **ratio** of the **current signal** to **the case when saturation is just starting**. Thus sine wave of peak 1.2 compared with a triangle with peak 2.0 will have a modulation depth of **m=0.6**.

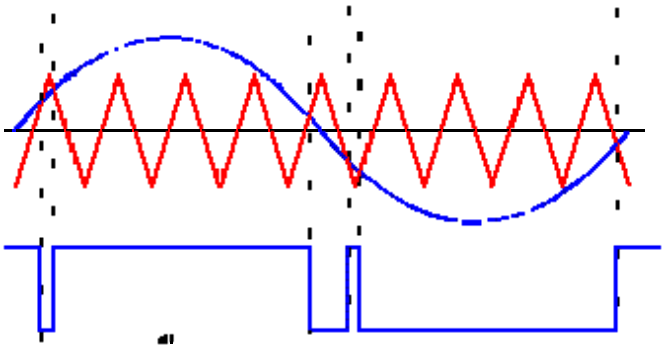


Fig. 6: Saturated Pulse Width Modulation

2.4.2 PWM Signal Generators

Testing status: Mixed. Some untested, some SPICE simulated.

2.4.2.1 1. Introduction

PWM, or **P**ulse **W**idth **M**odulation, is a method of controlling the amount of power to a load without having to dissipate any power in the load driver.

Imagine a 10W light bulb load supplied from a battery. In this case the battery supplies 10W of power, and the light bulb converts this 10W into light and heat. No power is lost anywhere else in the circuit. If we wanted to dim the light bulb, so it only absorbed 5W of power, we could place a resistor in series which absorbed 5W, then the light bulb could absorb the other 5W. This would work, but the power dissipated in the resistor not only makes it get very hot, but is wasted. The battery is still supplying 10W.

An alternative way is to switch the light bulb on and off very quickly so that it is only on for half of the time. Then the *average* power taken by the light bulb is still only 5W, and the average power supplied by the battery is only supplying 5W also. If we wanted the bulb to take 6W, we could leave the switch on for a little longer than the time it was off, then a little more average power will be delivered to the bulb.

This on-off switching is called PWM. The amount of power delivered to the load is proportional to the percentage of time that the load is switched on.

In the chapter on speed controllers on this site, there is an explanation why PWM signals are used to drive speed controllers. It is the same reason as for the light bulb example above.

2.4.2.2 2. The methods

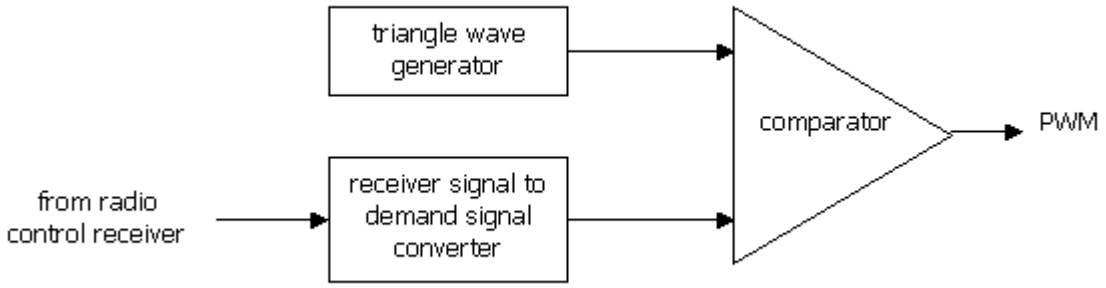
The PWM signals can be generated in a number of ways. There are several methods:

- 1. Analogue method
- 2. Digital method
- 3. Discrete IC
- 4. Onboard microcontroller

These will all be described.

2.4.2.2.1 2.1. Analogue method

A block diagram of an analogue PWM generator is shown below:

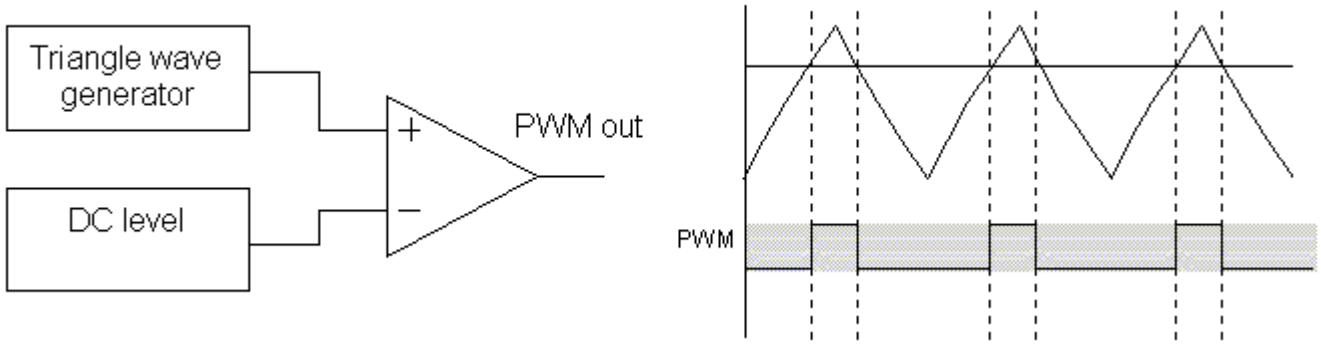


We will now go through each of these stages and work out how to implement them.

2.4.2.2.2 2.1.1. The comparator

We are starting at the output because this is the easy bit. The diagram below shows how comparing a ramping waveform with a DC level produces the PWM waveform that we require. The higher the DC level is, the wider the PWM pulses are. The DC level is the 'demand signal'.

The DC signal can range between the minimum and maximum voltages of the triangle wave.



When the triangle waveform voltage is greater than the DC level, the output of the op-amp swings high, and when it is lower, the output swings low.

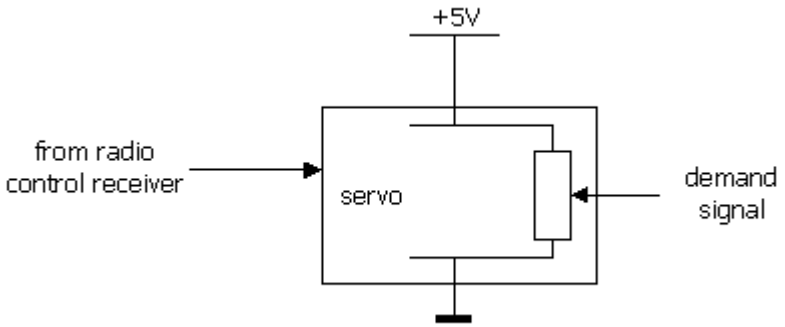
2.4.2.2.3 2.1.2. Detecting the demand signal

We need to convert the signal coming from the radio control receiver into a PWM demand signal. This can be achieved using a servo, or by using a circuit which decodes the signal from the receiver.

2.4.2.2.4 2.1.2.1. Using a servo

In this method, we want a PWM generator that will take a signal from a servo potentiometer (these signals will need to be taken out by wires from the servo body), and deliver a logic-level PWM output to the speed controller. When the servo potentiometer is at minimum, we want the PWM signal to be 100% off 0% on, and when the servo potentiometer is at maximum, we want the PWM signal to be 0% off 100% on. We also want the on percentage to be proportional to the potentiometer position.

The potentiometer generally has its 'top end' connected to a positive power supply, and its 'bottom end' connected to ground. Then as it rotates the voltage at its wiper changes linearly with wiper position.



2.4.2.2.5 2.1.2.2. Using the RxDetector circuit

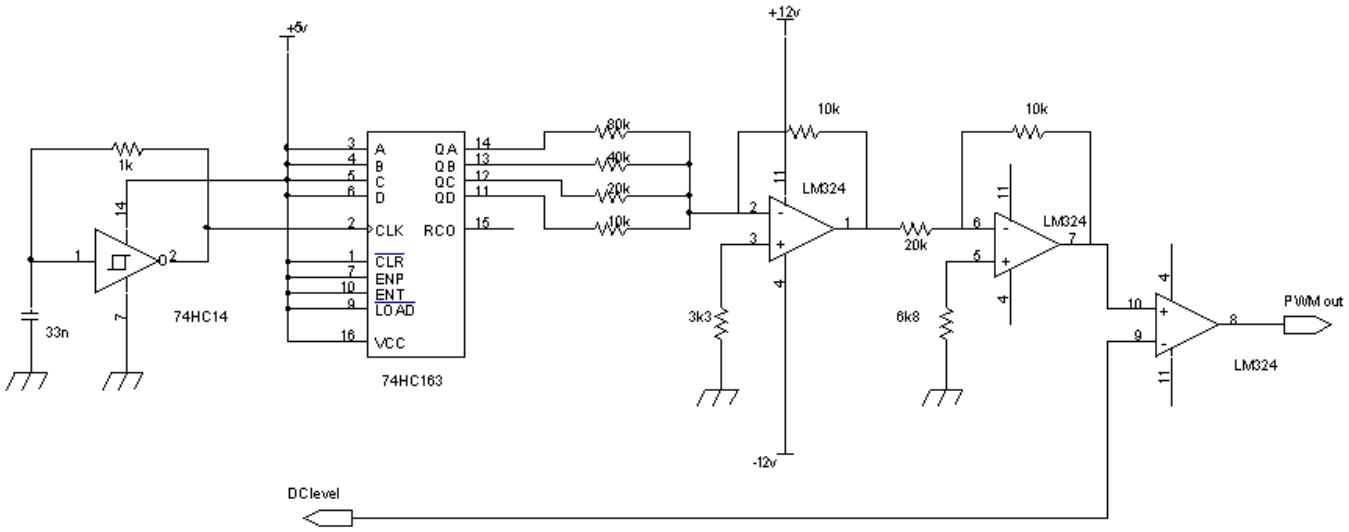
This is fully described in the RxDetector page.

2.4.2.3 2.1.3. Generating the triangle wave

There are a few ways of doing this:

2.4.2.3.1 2.1.3.1. Weighted resistor ladder on a counter

An example circuit for this is shown below. This uses a counter and weighted resistor ladder to generate the triangle wave (in fact it will generate a sawtooth, but you'll still get a PWM signal at the end of it). The actual resistor values which are unavailable (40k, 80k) can be made up with 20k resistors, or close approximations can be used, which may distort the sawtooth somewhat, but this shouldn't matter too much.



Click on the circuit diagram to open it in a new window.
http://homepages.which.net/~paul.hills/Circuits/PwmGenerators/PWMgenerator.gif

The 74HC14 is a Schmitt input inverter, which is connected to act as a simple oscillator. The frequency of oscillation is roughly

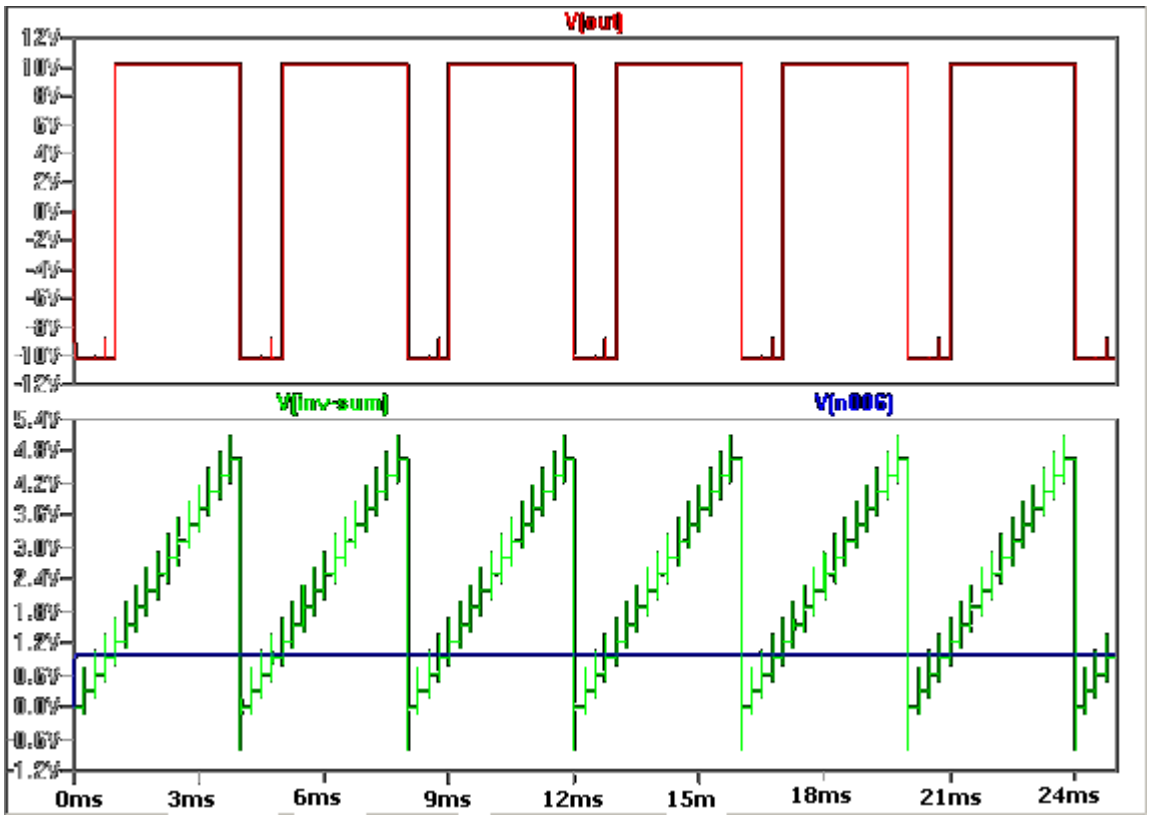
$$f_{osc} = \frac{1}{2\pi RC}$$

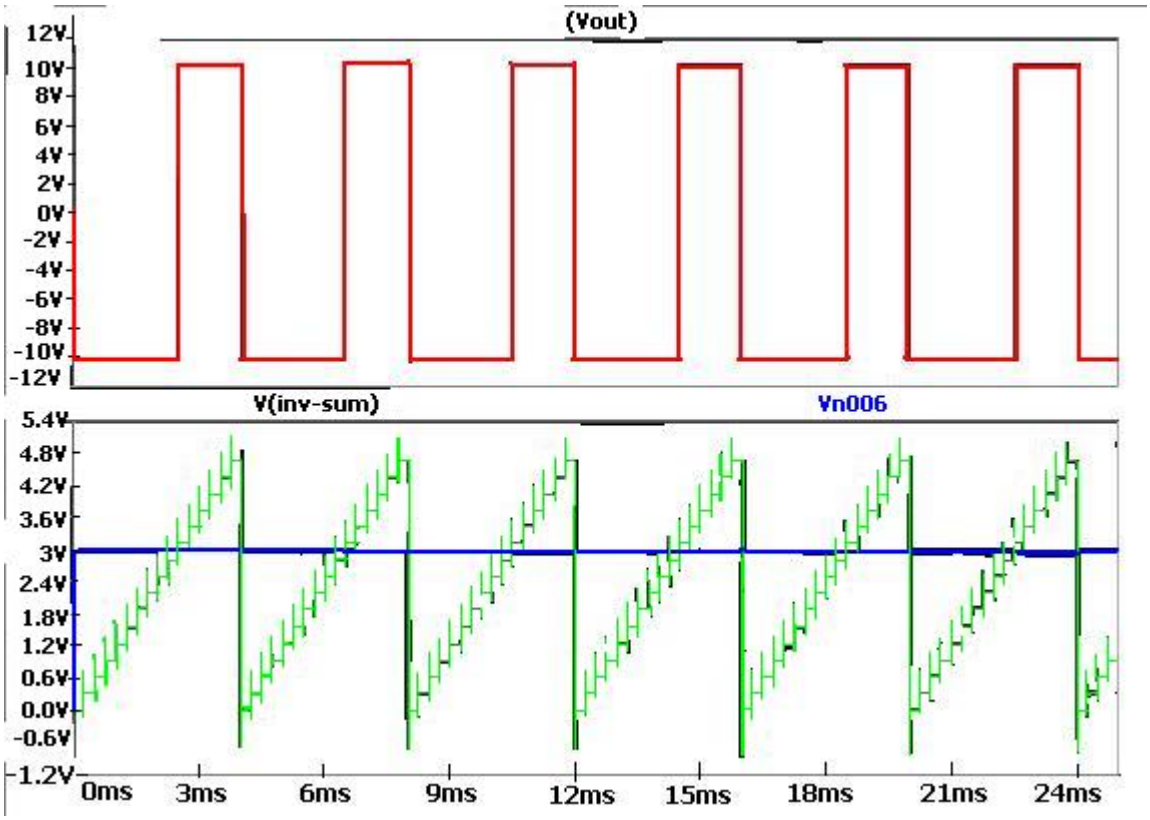
but it doesn't matter a great deal within a few tens of percent. This square wave generated feeds the 74HC163 binary 4-bit counter. All the preset and clear inputs of this are disabled,

so the outputs, Q_A to Q_D just roll around the binary sequence 0000 to 1111 and rollover to 0000 again. These outputs, which swing from 0v to +5v are fed into a binary weighted summer amplifier, the leftmost LM324 op amp section with the 80k, 40k, 20k and 10k resistors. The output voltage of this amplifier depends on the counter count value and is shown in the table below as Amp1 output. The op amp following this just multiplies the voltage by -½, to make the voltage positive, and bring it back within logic voltage levels, see the Amp2 output column in the table.

Counter value	Binary value	Amp1 output (Volts)	Amp2 output (Volts)
0	0000	0	0
1	0001	-0.625	0.3125
2	0010	-1.25	0.625
3	0011	-1.875	0.9375
4	0100	-2.5	1.25
5	0101	-3.125	1.5625
6	0110	-3.75	1.875
7	0111	-4.375	2.1875
8	1000	-5	2.5
9	1001	-5.625	2.8125
10	1010	-6.25	3.125
11	1011	-6.875	3.4375
12	1100	-7.5	3.75
13	1101	-8.125	4.0625
14	1110	-8.75	4.375
15	1111	-9.375	4.6875

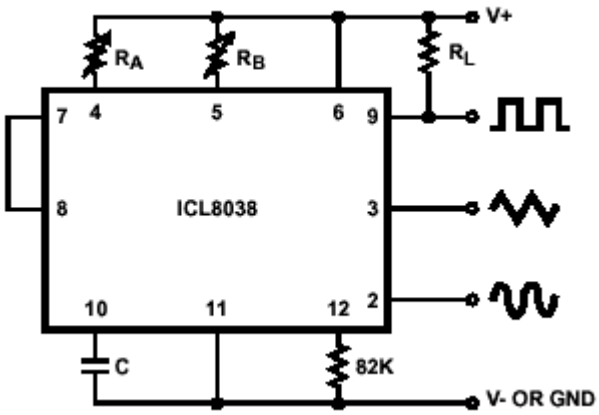
The results of two SPICE simulations are shown below. The first is with the DC threshold level set at +1V, and the second with it set at +3V. The blue line is the threshold level, the green line is at the +ve input of the rightmost comparator, and the red waveform is the output. The difference in PWM ratio can be clearly seen.


V(out)
V(inv-sum)
V(n006)
0ms
3ms
6ms
9ms
12ms
15m
18ms
21ms
24ms


(Vout)
12V
10V
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
-12V
V(inv-sum)
Vn006
5.4V
4.8V
4.2V
3.6V
3V
2.4V
1.8V
1.2V
0.6V
0.0V
-0.6V
-1.2V
0ms
3ms
6ms
9ms
12ms
15ms
18ms
21ms
24ms

2.4.2.3.2 2.1.3.2. Waveform generator ICs

ICs specially designed for generating triangle waves are available. Perhaps the most commonly know is the ICL8038, which is quite long in the tooth now but is still perfectly adequate. A circuit for generating a suitable triangle wave is shown below.



Set R_A equal to R_B for a regular triangle wave (equal rising and falling edges). The frequency of the triangle wave is then given by the equation:

$$f = \frac{0.33}{R_A C}$$

The capacitor value should be chosen at the upper end of its possible range. The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (+/-5V to +/-15V). The triangle wave swings from 1/3 of the supply voltage up to 2/3 of the supply voltage, so on a +12V single supply it would swing from 4V to 8V.
The 8038 is also second sourced by Exar

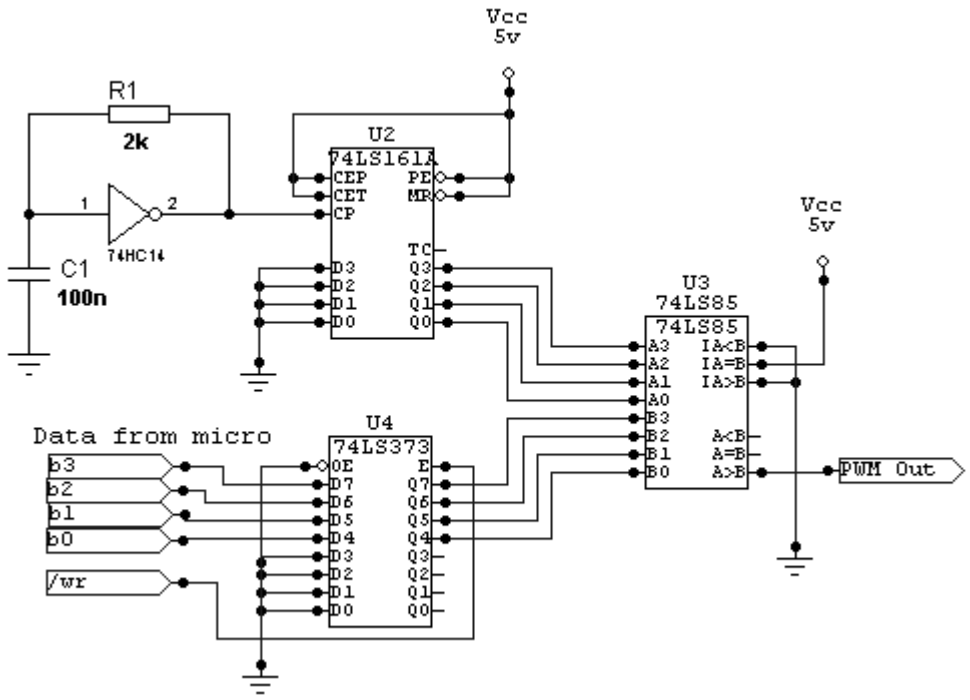
2.4.2.4 2.2. Digital methods

The digital method involves incrementing a counter, and comparing the counter value with a pre-loaded register value, or a value set by an ADC. It is basically a digital version of the analogue method above.

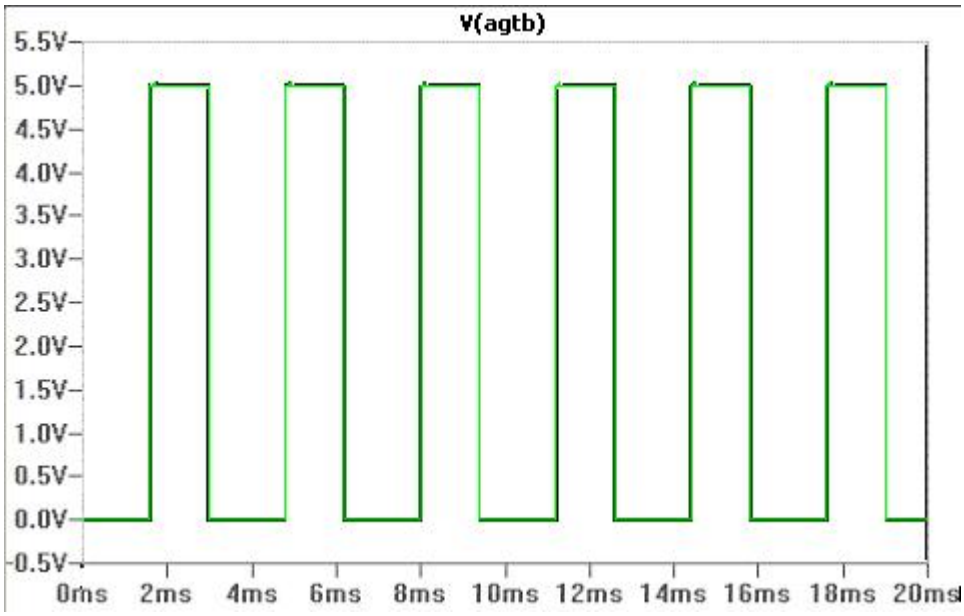
2.4.2.5 2.2.1. Digital register method

The register must be loaded with the required PWM level by a microcontroller. This may be replaced by a simple ADC if the level must be controlled by an analogue signal (as it would from a radio control servo).
Below is an example circuit using the digital comparison method when a microcontroller is available to set the 4-bit digital register value. A write strobe is required from the micro to latch the 4 data bits into the register. The 74HC161 counter is free-running, the frequency being set by the 74HC14 oscillator section, where it is roughly f = 1/(6.3RC). The resulting frequency of the PWM signal will be 16 times less than this counter clock frequency, since it requires 16 pulses to complete one "revolution" of the counter. With R=2k and C=1nF this

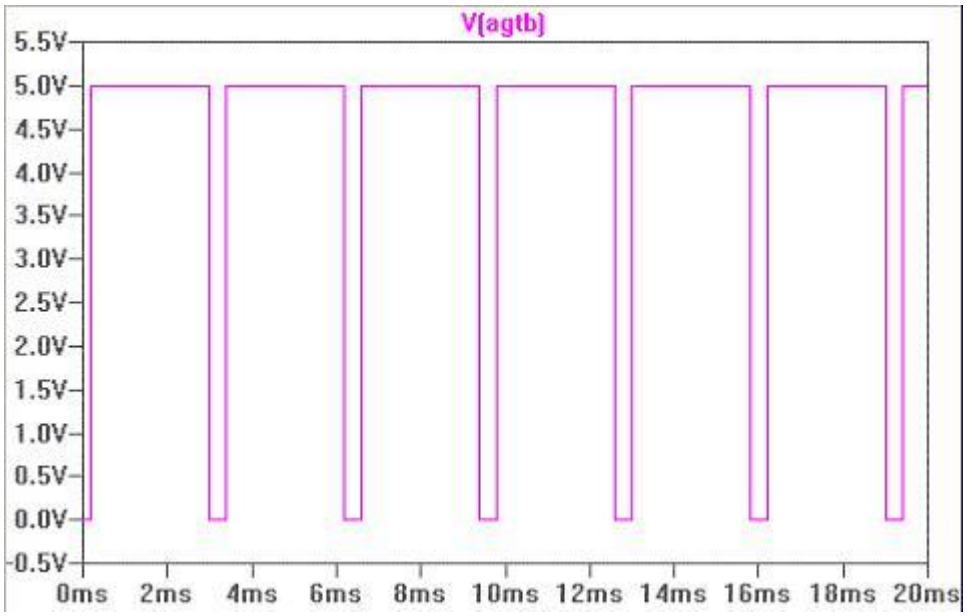
results in a counter frequency of approximately 80kHz which will result in a PWM signal frequency of 5kHz.
The 74HC85 "Greater Than" output will go high when the counter value exceeds the value set in the register. Because this circuit is all 4-bit, there will be 16 discrete levels of mark-space ratio, which is perfectly adequate for our requirements.



Click on the circuit diagram to open it in a new window.
With the threshold value (the value stored in the 74HC373) equal to 8 (i.e. Q7=1 and Q6=Q5=Q4=0), the following (Spice simulation) waveform is generated:

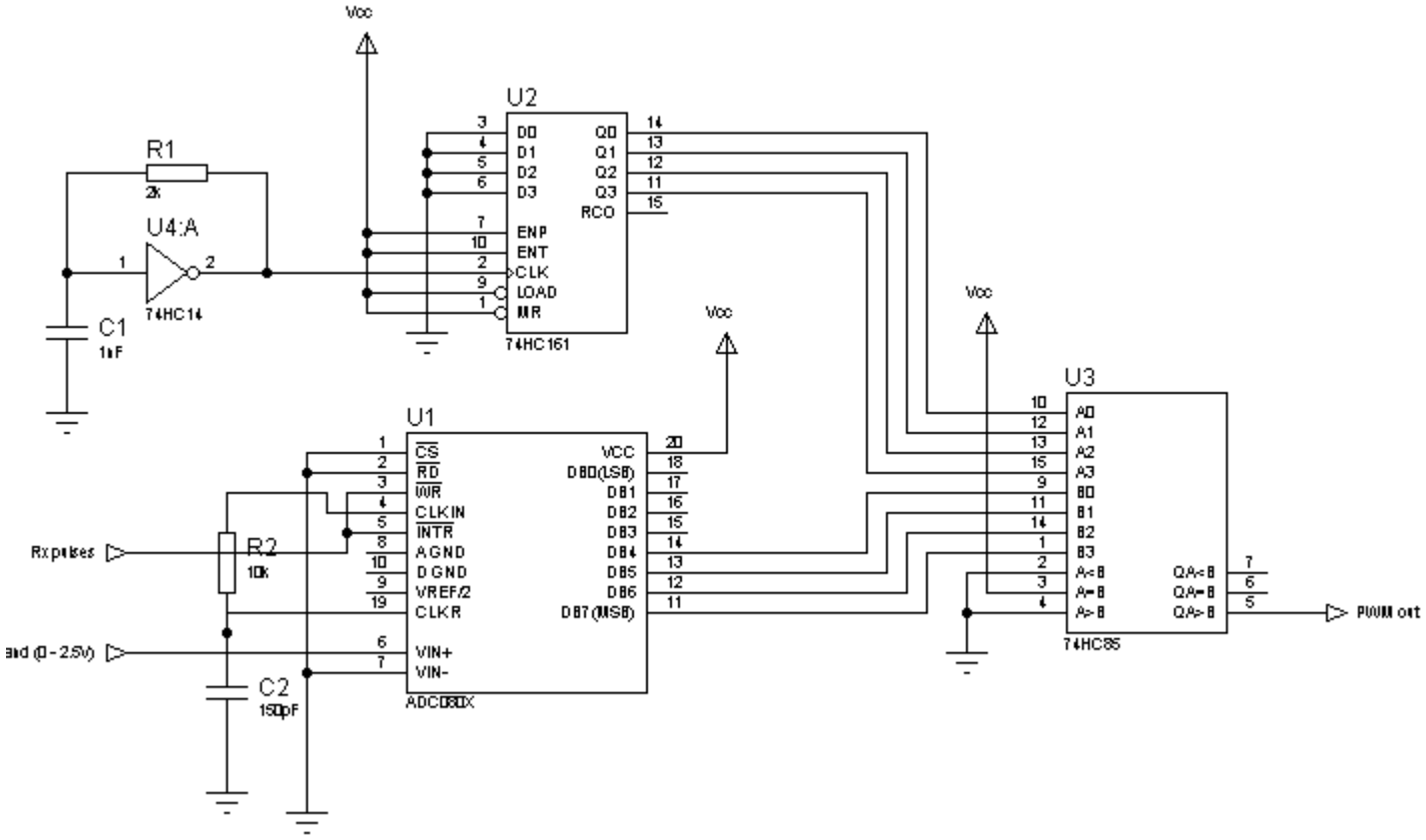


and with the threshold value equal to 1 (i.e. Q7=Q6=Q5=0 and Q4=1), this waveform is generated:



2.4.2.6 2.2.2. Digital ADC method

This circuit is basically the same as the previous one, except the demand value that is compared is generated by the National Semiconductor ADC0804 basic 8-bit ADC converter. Since this is an 8-bit ADC, the bottom 4 bits are left unused. The converter is configured to automatically clock itself, with a conversion speed governed by R2 and C2 in the circuit. Here, the conversion rate is fixed at 640kHz which is recommended in the datasheet.
The demand input range is 0 to 2.5V by default, and this may be set by a Receiver Decoder circuit, or by any other means such as a 6V servo potentiometer voltage divided by 2.4.
Although the ADC is self clocking, it does require at least one single pulse on the /WR input to guarantee correct startup. This doesn't have to be a single pulse, it may be recurrent, so the pulse from the radio control receiver which repeats every 20ms are adequate. The complete circuit is shown below.



Click on the circuit diagram to open it in a new window.

2.4.2.7 2.2.3. Including the Receiver Decoder

In the Receiver Decoder page, a digital circuit was presented which decoded the pulse from the RC receiver into a 4-bit word. That circuit can be merged with the circuit of section 2.2.1 above to arrive at a completely digital solution to PWM generation. The Receiver Decoder circuit replaces U4 of the circuit of section 2.2.1.

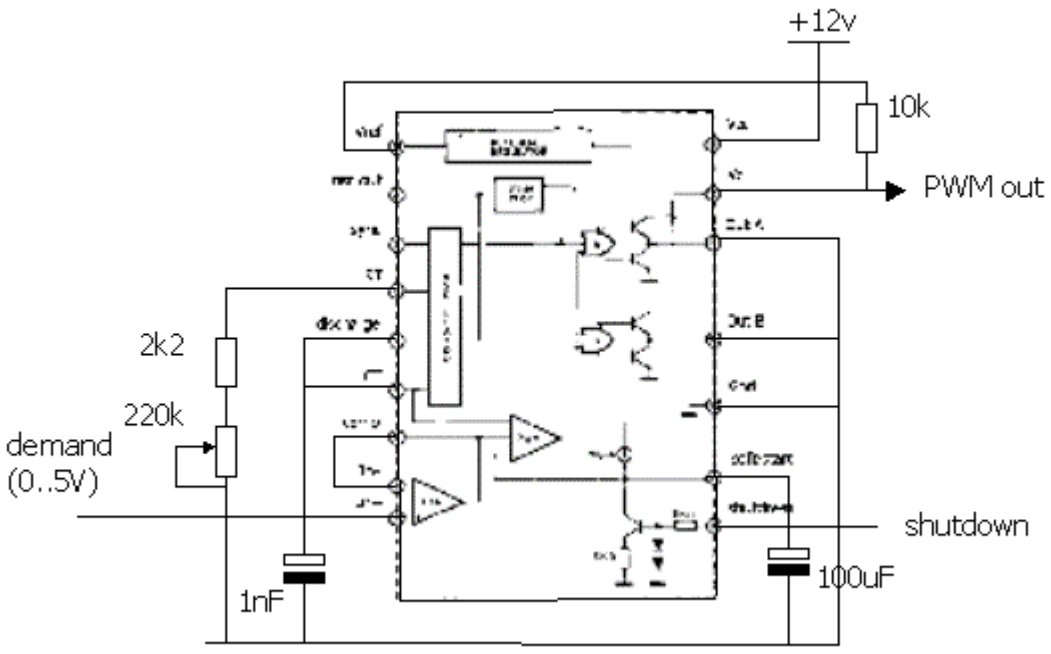
2.4.2.8 2.3. PWM generator chips

There are ICs available which convert a DC level into a PWM output. Many of these are designed for use in switch mode power supplies. Unfortunately, the devices designed for switch mode power supplies tend not to allow the mark-space ratio to alter over the entire 0 - 100% range. many limit the maximum to 90% which is effectively limiting the power you can send to the motors. Devices designed as pulse generators should allow the whole range to be used. Examples are:

Manufacturer	IC	Normal use	Comment
ST	SG1524 SG3525A	SMPS	May operate at up to 100% duty cycle
Maxim	MAX038	Signal generation	PWM output only between 15% and 85%. Generates triangle & sine waves too.
Atmel	U2352B	PWM Generator for speed control of portable tools	Includes integrated current limiting circuitry for output MOSFETs.
TI	TL494	SMPS	Max 90% duty cycle
TI	UC2638	PWM generator for motor control	Provides many other features for DC motor speed control. Note there are many other TI motor control devices listed here.

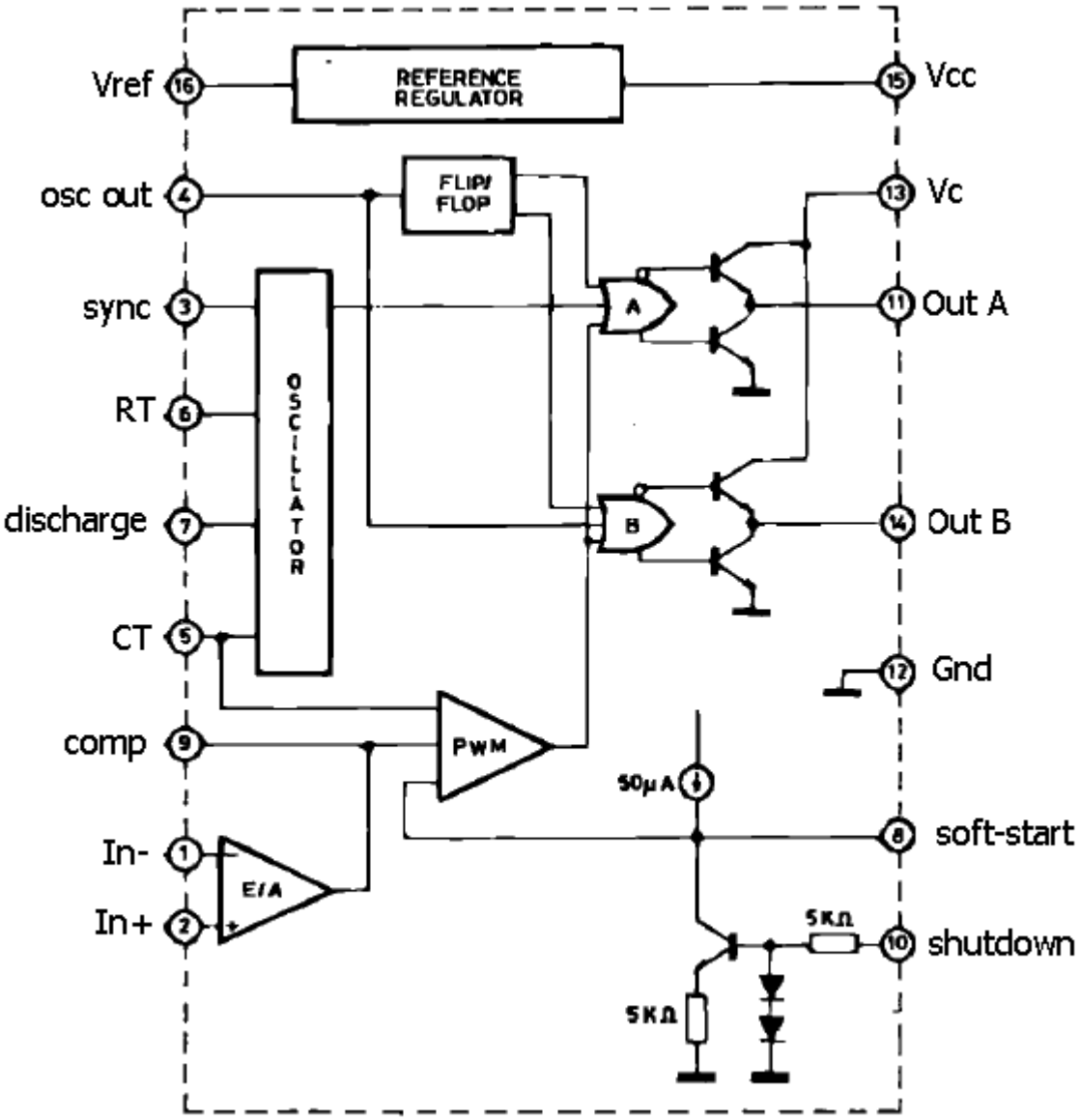
Alternatively, a MOSFET driver which includes a PWM generator can be used. I know of only one which is not yet released! The SGS Thomson TD340.

I will present a design using the SG3525A. Thanks to Clive Sinclair (not that one!) and Mark Case for this circuit:



2.4.2.9 Circuit description

This IC is designed for use in switched mode power supplies, but can be configured to work nicely for our requirements. To explain the function of this circuit it is helpful to look at the innards of the chip, shown below:



The speed demand signal is input at pin 2, the op amp non-inverting input. The internal op amp is wired as a simple unity gain follower, and the demand signal is then applied to the PWM comparator. This compares the demand level with the oscillator output, in the same fashion as that shown in section 2.1.1.

The frequency of the oscillator, and therefore the PWM signal produced, is governed by the value of the resistor to ground on the R_T pin. The sync and osc out pins are not required for our purposes.
The output stage is a little odd, since it is designed for driving bipolar transformers in SMPS circuits. However, we can wire it so it produces a simple single PWM waveform. By not using the bottom transistor of the totem-pole output stages on both OutA and OutB outputs, tying OutA and OutB to ground, attaching a pull-up resistor to the Vc pin, then the bottom transistors of the output stages simply switch the Vc pin to ground, and the signal at the Vc pin is our required PWM signal.
The IC also has two protection mechanisms for use in SMPS circuits which we can also make use of. The soft start feature prevents the output from saturating at 100% ratio when the chip is powering up. This is useful for us as it stops the motors from being driven as our circuits are powering up. The Shutdown input is an active-high input that immediately shuts down the outputs, and resets the soft-start feature. This can be used by current-limiting circuitry to turn off the power MOSFETs in the speed controller, and the soft-start will back-off the PWM while the problem can be addressed by the driver.

2.4.2.10 2.4. Onboard microcontroller

If you have a microcontroller on the robot, this may be able to generate the waveform, although if you have more than a couple of motors, this may be too much of a load on the microcontroller's resources. So if you have chosen to use an onboard microcontroller, then as part of your selection process, include whether it has PWM outputs. If it has this can greatly simplify the process of generating signals. The Hitachi H8S series has up to 16 PWM outputs available, but many other types have two or three.

2.4.3 Devices used in these circuits

The following devices were used in this circuit. Click on the manufacturer's name to go to their web site, or the device name to go to the device datasheet.

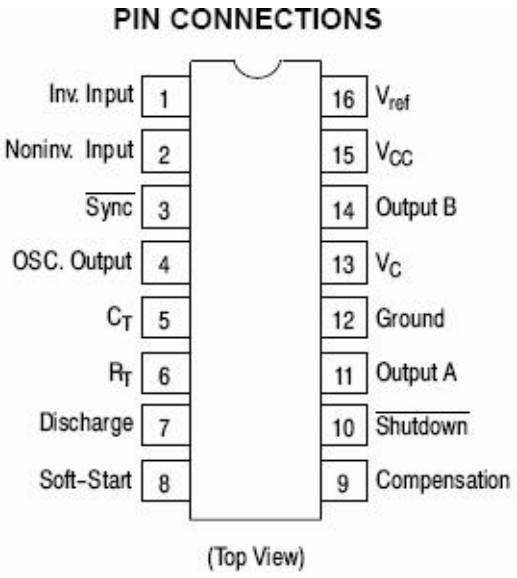
Manufacturer	Device
SGS Thompson	SG3525A SMPS controller
National Semiconductor	ADC0804 8-bit ADC
	LM324 Dual op amp
Intersil	ICL8038 Waveform generator
Philips Semiconductors	74HC00 Quad NAND gate
	74HC14 Schmitt input inverter
	74HC85 4-bit comparator
	74HC161 4-bit synchronous counter
	74HC163 4-bit synchronous counter
	74HC373 Octal transparent latch
Welwyn	0.1% precision fixed resistor e.g. RS part no 165-769

Back to circuits index (http://homepages.which.net/~paul.hills/Circuits/Circuits.html)
Back to main index (http://homepages.which.net/~paul.hills/index.html)

2.5 Circuitos de PWM.

2.5.1 SG3525A Pulse Width Modulator Control Circuit

The **SG3525A** pulse width modulator control circuit offers improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on−chip +5.1 V reference is trimmed to _1% and the error amplifier has an input common−mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the CT and Discharge pins. This device also features built−in soft−start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft−start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft−start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft−start capacitor when VCC is below nominal. The output stages are totem−pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off−state.



- 8.0 V to 35 V Operation
- 5.1 V _1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse−by−Pulse Shutdown
- Dual Source/Sink Outputs: _400 mA Peak

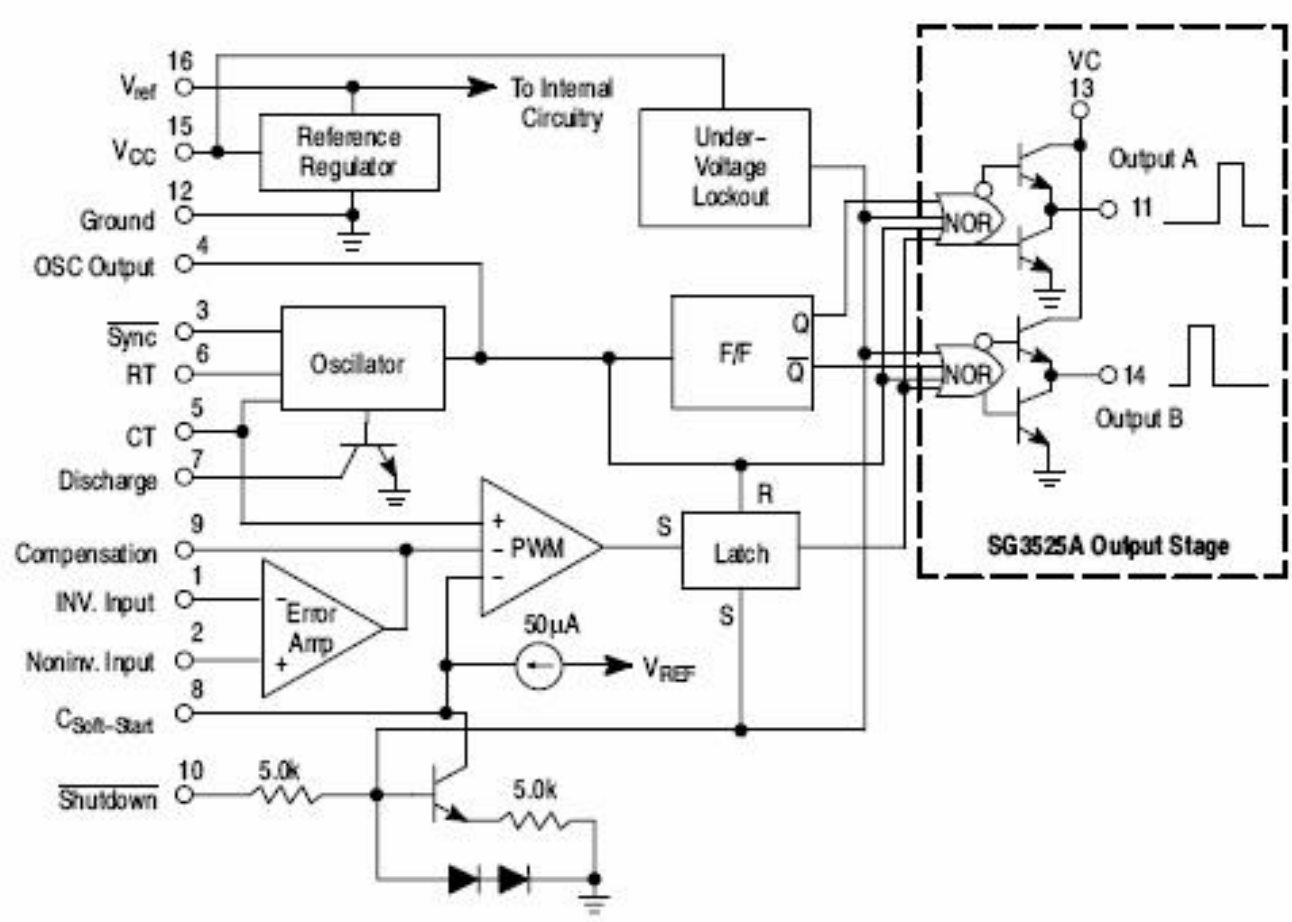
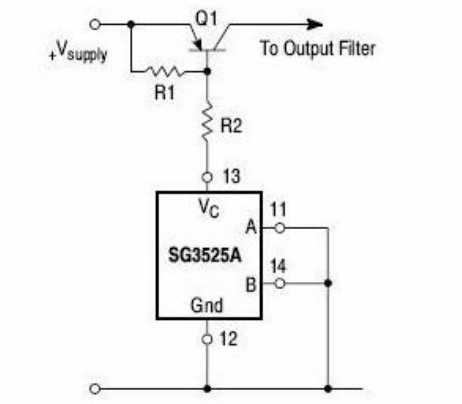
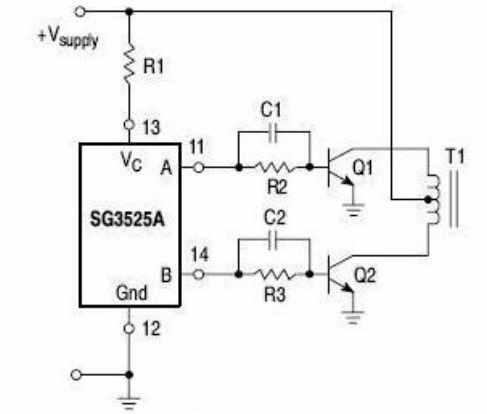


Figure 1 Representative Block diagram.



For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

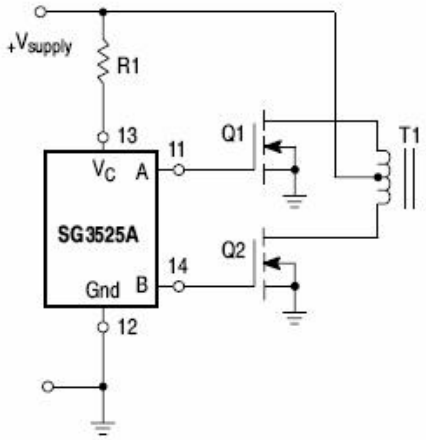
Figure 10 Single ended supply.



In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

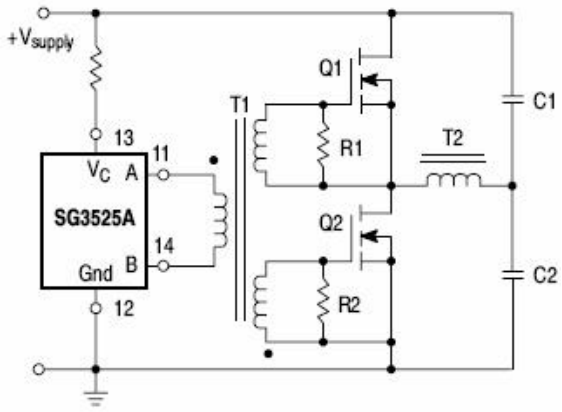
Figure 11 Push-Pull configuration.

Some applications for the SG3525.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 12. Driving Power FETS



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

Figure 13. Driving Transformers in a Half–Bridge Configuration

Applications for the SG3525.

2.5.2 TL494 PULSE-WIDTH-MODULATION CONTROL CIRCUITS

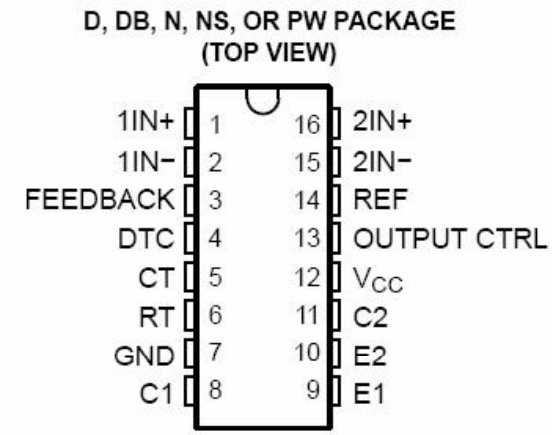
FEATURES

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

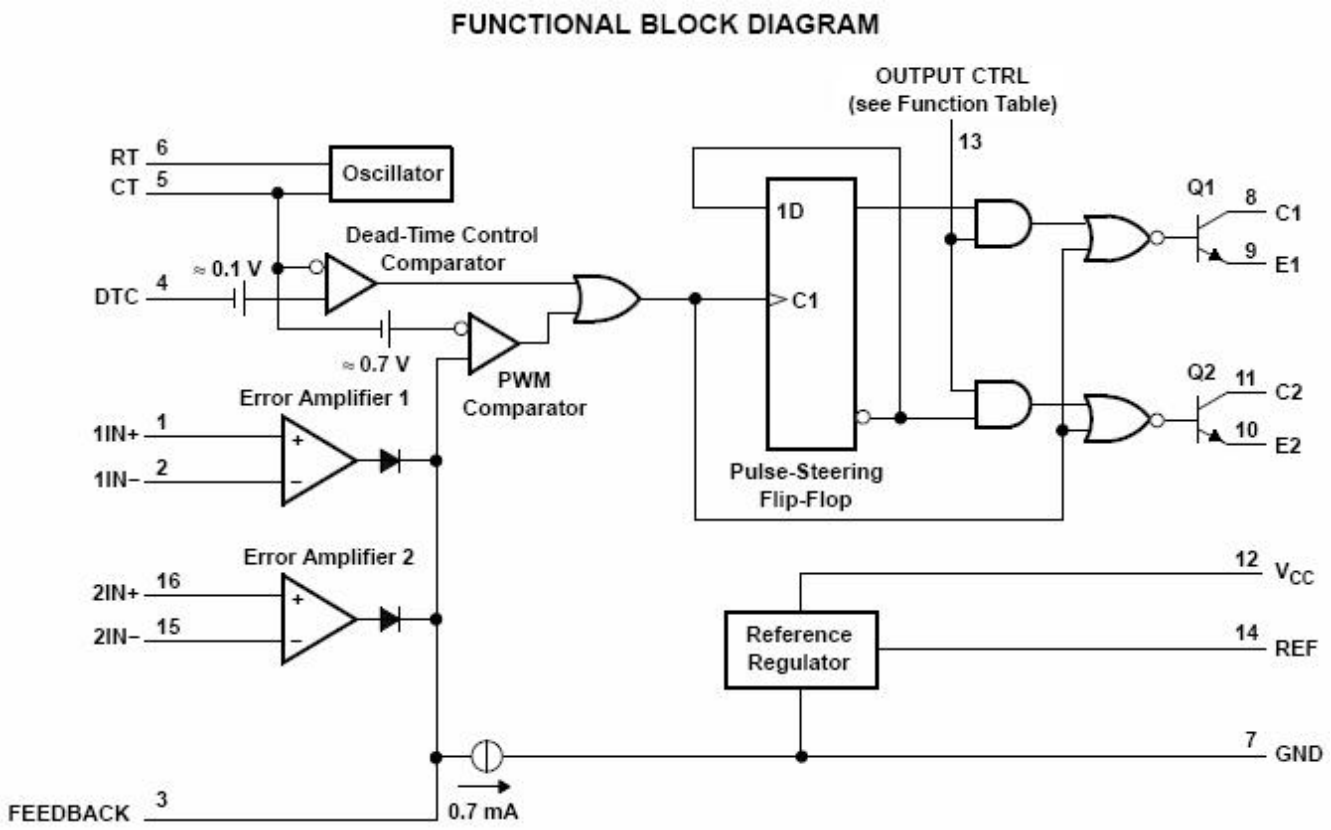
DESCRIPTION

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application. The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits. The error amplifiers exhibit a common-mode voltage range from –0.3 V to VCC – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control

function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation. The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from –40°C to 85°C.



TL494 pinout.



Functional block diagram.

2.5.3 UC2638 Advanced PWM Motor Controller

Unitrode Products from Texas Instruments

FEATURES

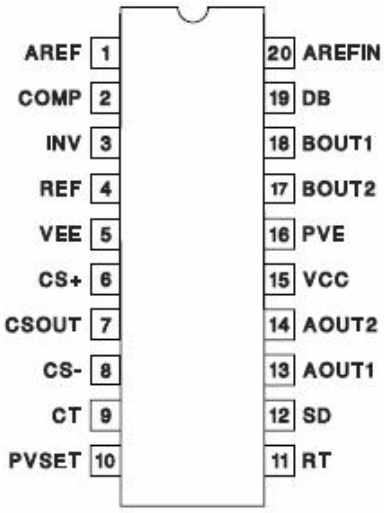
- Single or Dual Supply Operation
- Accurate High Speed Oscillator
- Differential X5 Current Sense Amplifier
- Bidirectional Pulse-by-Pulse Current Limiting
- Programmable Oscillator Amplitude and PWM Deadband
- Dual 500mA Totem Pole Output Drivers
- Dual 60V, 50mA Open Collector Drivers
- Undervoltage Lockout

DESCRIPTION

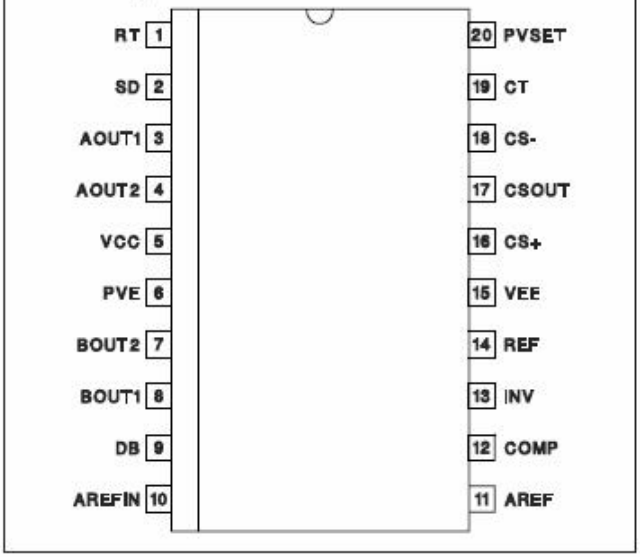
The **UC2638** family of integrated circuits are advanced pulse width modulators intended for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. Similar in architecture to the UC2637, all necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity. Key features of the UC2638 include a programmable high speed triangle oscillator, a 5X differential current sensing amplifier, a high slew rate error amplifier, high speed PWM comparators, and two 50mA open collector as well as two □500mA totem pole output stages. The individual circuit blocks are designed to provide practical operation to switching frequencies of 500kHz. Significant improvements in circuit speed, elimination of many external programming components, and the inclusion of a differential current sense amplifier, allow this controller to be specified for higher performance applications, yet maintain the flexibility of the UC2637. The current sense amplifier in conjunction with the error amplifier can be configured for average current feedback. The additional open collector outputs provide a drive signal for the highside switches in a full bridge configuration. The programmable AREFIN pin allows for single or dual supply operation. Oscillator ramp amplitude and PWM deadband are programmable by tapping a voltage divider off the 5V reference to the appropriate programming input (PVSET or DB). Additional features include a precision externally available 5V reference, undervoltage lockout, pulse-by-pulse peak current limiting, and a remote shutdown port. The UC1638 family is available in the 20 pin N, DW and J packages. Consult the factory for other packaging options.

CONNECTION DIAGRAMS

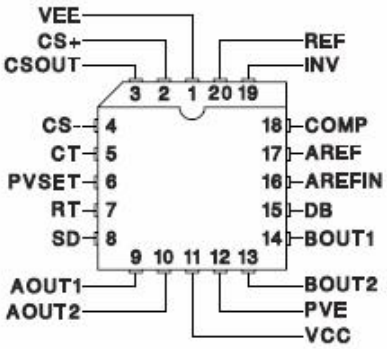
DIL-20 (Top View)
N Package



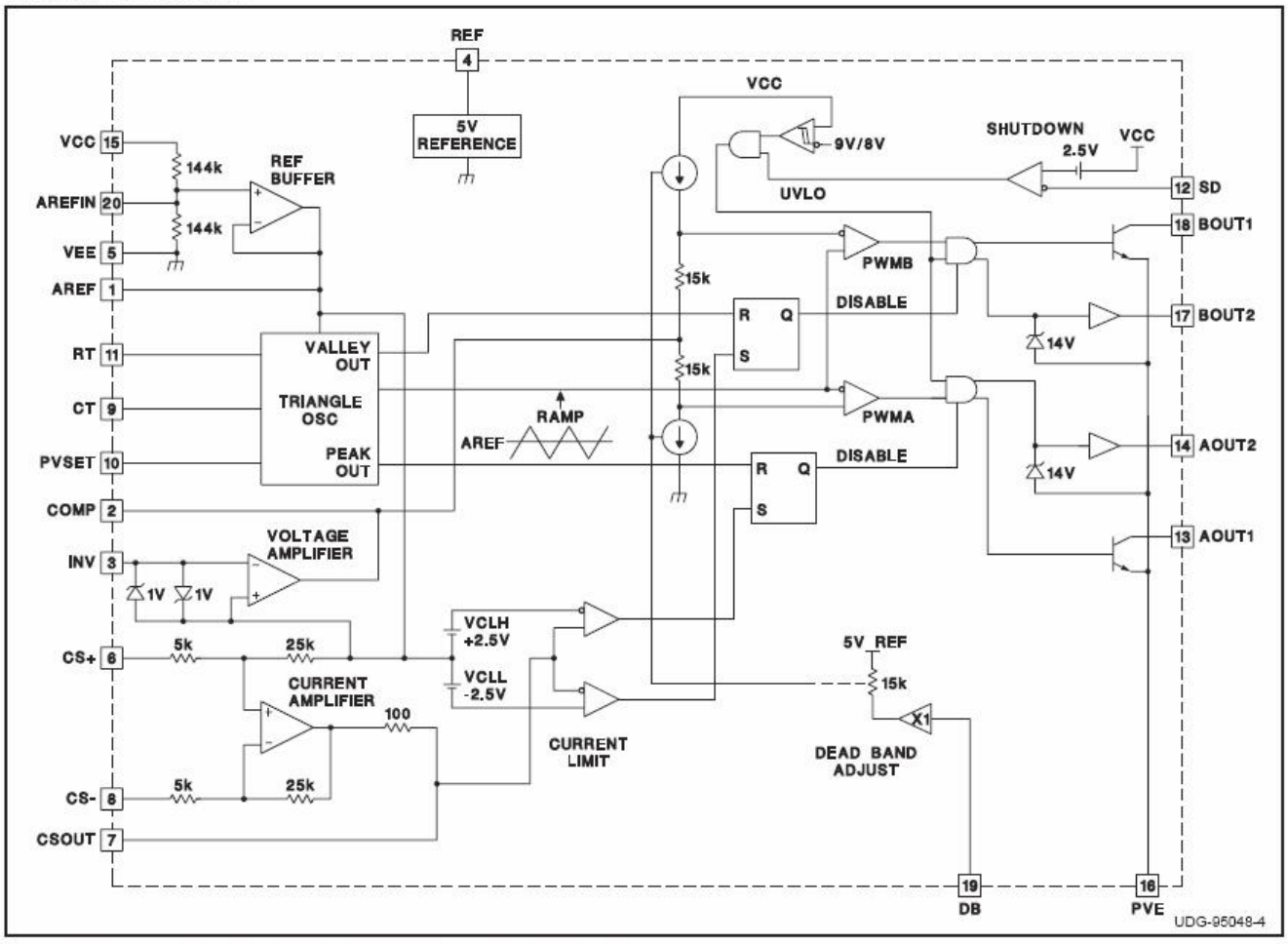
SOIC-20 (Top View)
DW Package



PLCC-20 (Top View)
Q Package



BLOCK DIAGRAM



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APPLICATION INFORMATION

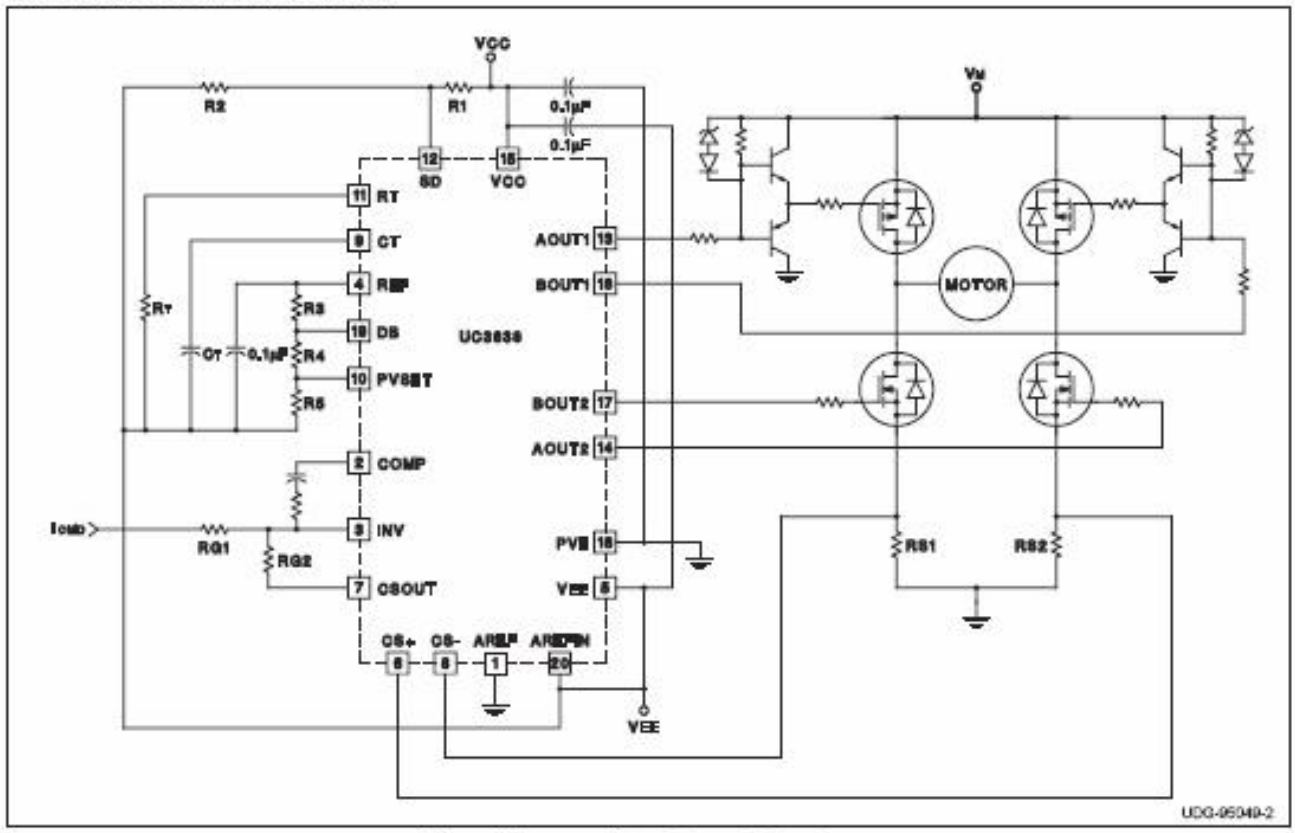


Figure 1. Average Motor Current Control Loop

Motor control with UC2638

2.5.4 MAX038 High-Frequency Waveform Generator

DESCRIPTION

The MAX038 is a high-frequency, precision function generator producing accurate, high-frequency triangle, saw-tooth, sine, square, and pulse waveforms with a minimum of external components. The output frequency can be controlled over a frequency range of 0.1Hz to 20MHz by an internal 2.5V band gap voltage reference and an external resistor and capacitor. The duty cycle can be varied over a wide range by applying a ±2.3V control signal, facilitating pulse-width modulation and the generation of saw-tooth waveforms. Frequency modulation and frequency sweeping are achieved in the same way. The duty cycle and frequency controls are independent.

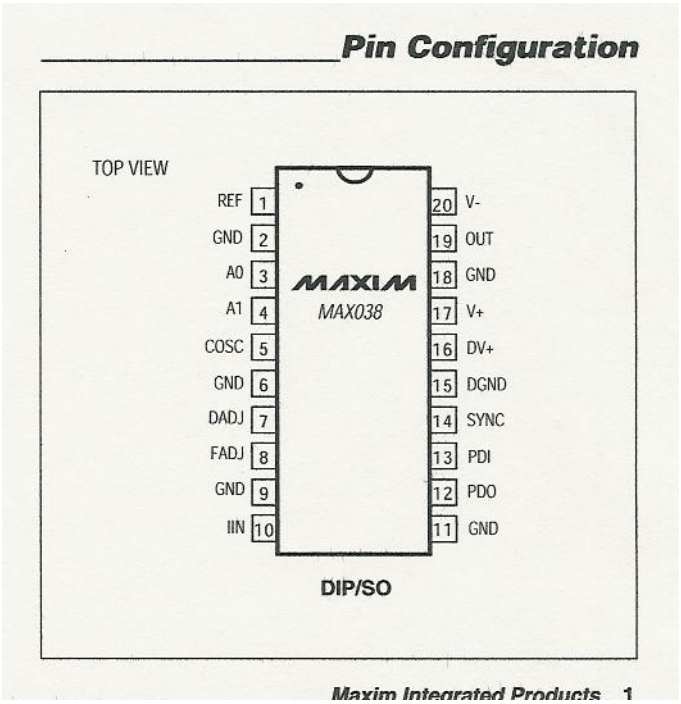
Sine, square, or triangle waveforms can be selected at the output by setting the appropriate code at two TTL-compatible select pins. The output signal for all waveforms is a $2V_{P-P}$ signal that is symmetrical around ground. The low-impedance output can drive up to ±20mA. The TTL-compatible SYNC output from the internal oscillator maintains a 50% duty cycle—regardless of the duty cycle of the other waveforms—to synchronize other devices in the system. The internal oscillator can be synchronized to an external TTL clock connected to PDI.

APPLICATIONS

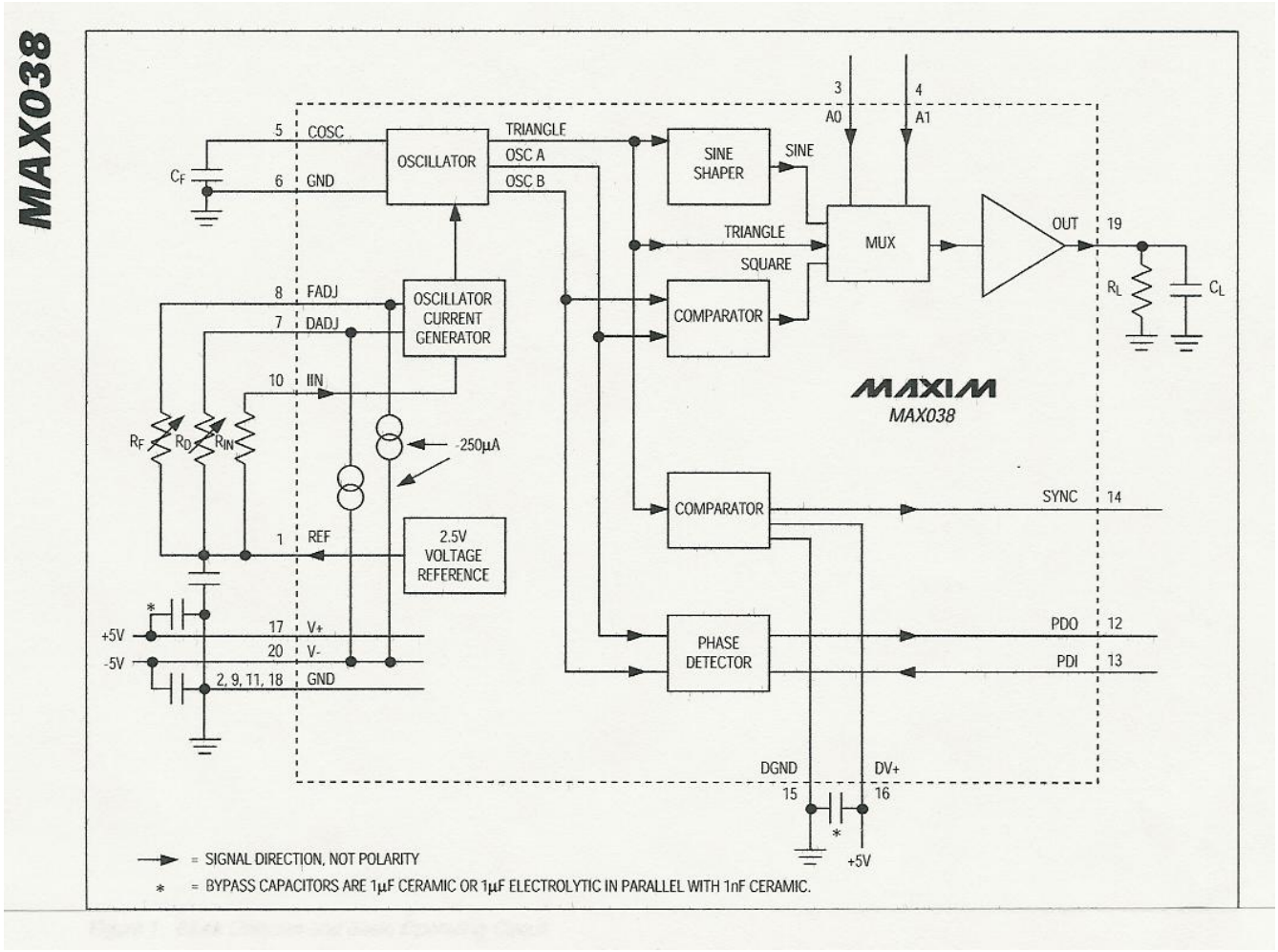
- 0.1Hz to 20MHz Operating Frequency Range
- Triangle, Saw-tooth, Sine, Square, and Pulse Waveforms
- Independent Frequency and Duty-Cycle Adjustments
- 350 to 1 Frequency Sweep Range
- 15% to 85% Variable Duty Cycle
- Low-Impedance Output Buffer: 0.1Ω
- Low 200ppm/°C Temperature Drift

KEY FEATURES

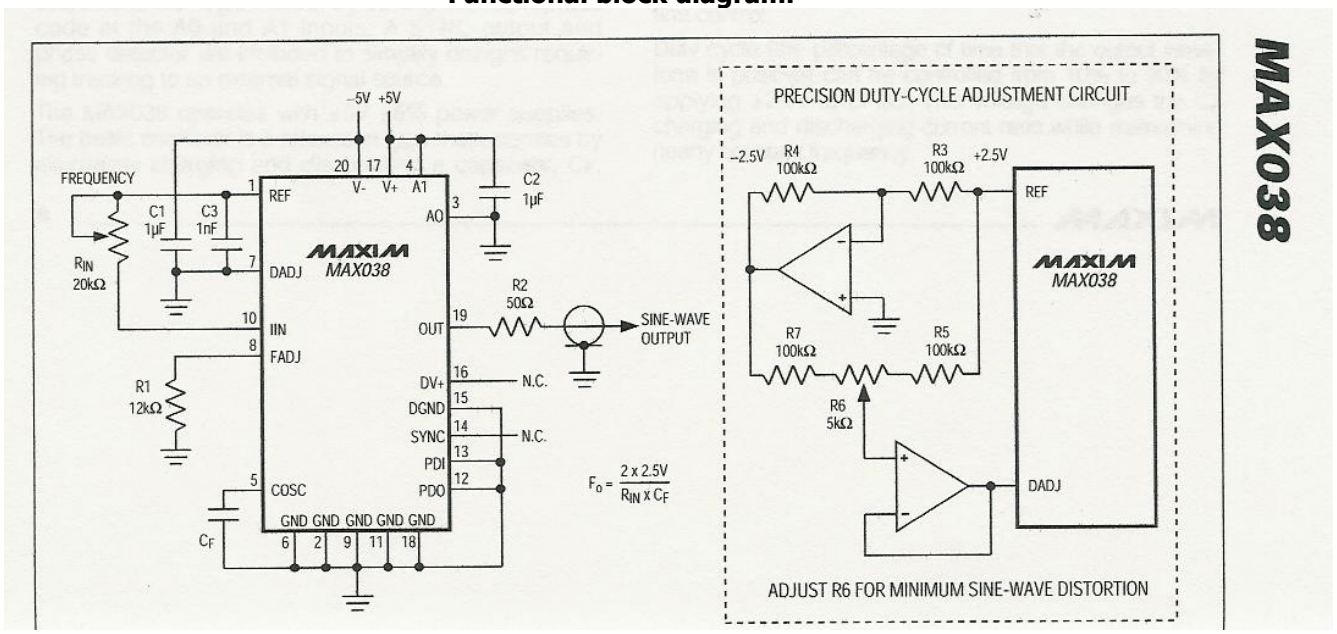
- Frequency Modulators
- Frequency Synthesizer
- FSK Generator—Sine and Square Waves
- Phase-Locked Loops
- Precision Function Generators
- Pulse-Width Modulators
- Voltage-Controlled Oscillators



MAX038 Pinout.



Functional block diagram.



Sine wave generator.

2.6 Estructura y ecuaciones de diseño.(1.4)

Design Example

The following design example uses the TL494 to create a 5-V/10-A power supply. This design is based on the following parameters:

VO = 5 V
VI = 32 V
IO = 10 A
fOSC = 20-kHz switching frequency
VR = 20-mV peak-to-peak (VRIPPLE)
ΔIL = 1.5-A inductor current change

Input Power Source

The 32-V dc power source for this supply uses a 120-V input, 24-V output transformer rated at 75 VA. The 24-V secondary winding feeds a full-wave bridge rectifier followed by a current-limiting resistor (0.3 Ω) and two filter capacitors (see Figure 34).

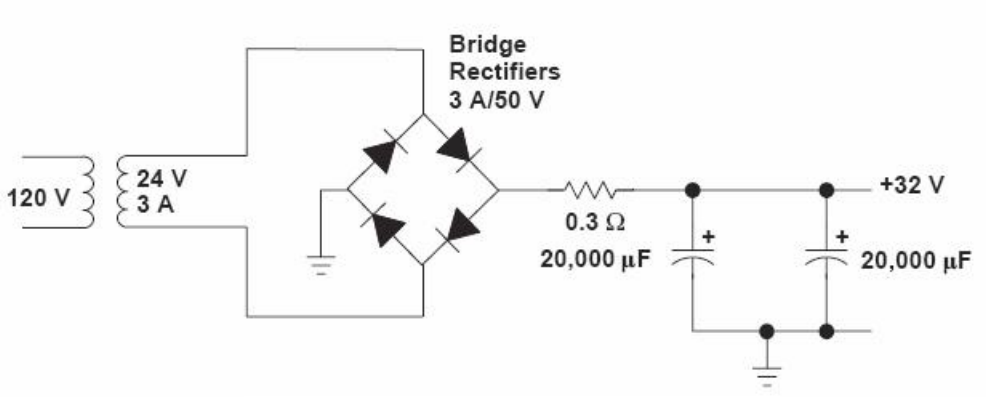


Figure 34. Input Power Source

The output current and voltage are determined by equations 6 and 7:

$$V_{RECTIFIER} = V_{SECONDARY} \times \sqrt{2} = 24\ V \times \sqrt{2} = 34\ V \quad (6)$$

$$I_{RECTIFIER(AVG)} \sim (V_O/V_I) \times I_O \sim 5\ V/32\ V \times 10\ A = 1.6\ A \quad (7)$$

The 3-A/50-V full-wave bridge rectifier meets these calculated conditions. Figure 35 shows the switching and control sections.

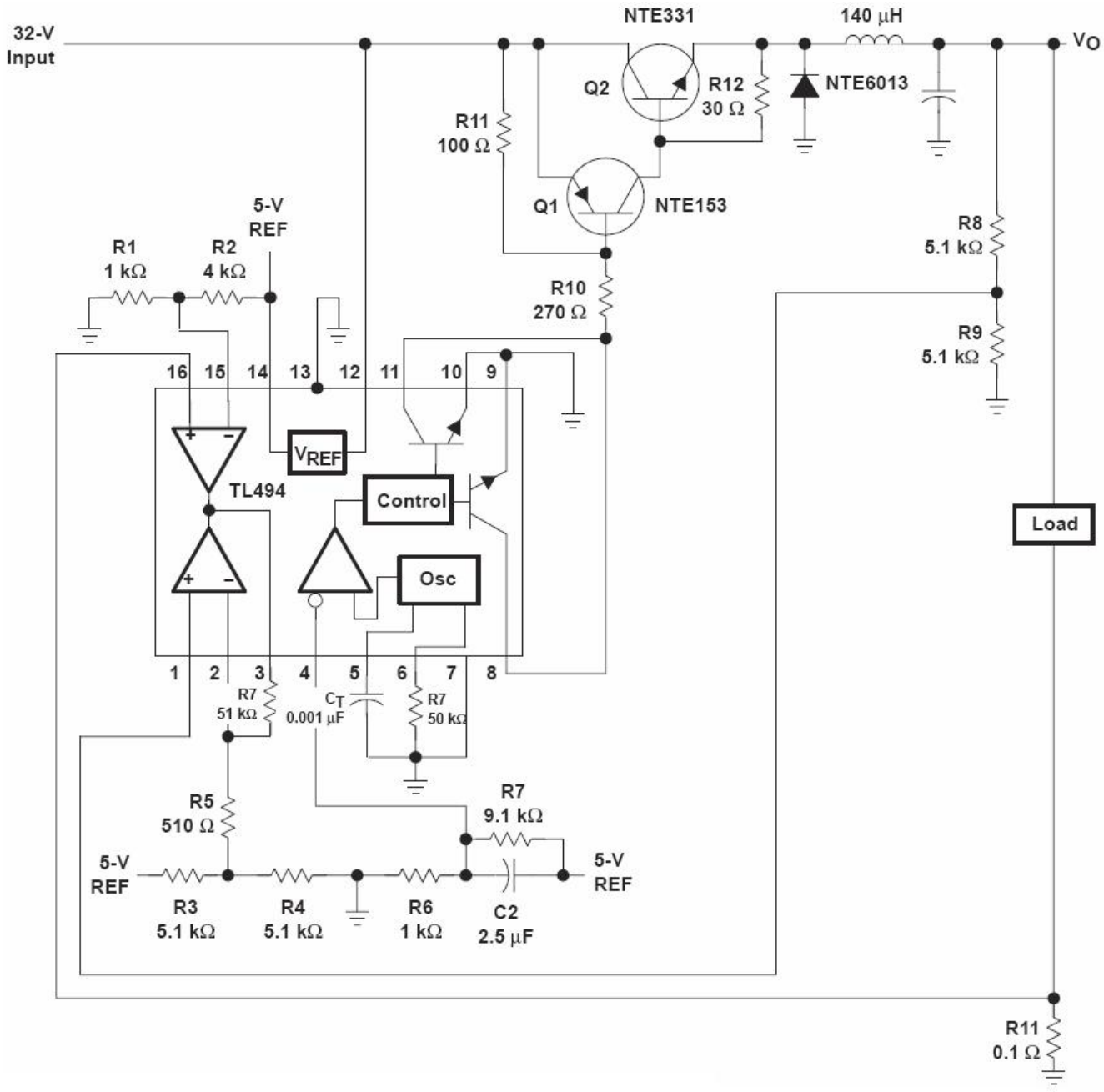


Figure 35. Switching and Control Sections

Control Circuits

Oscillator

Connecting an external capacitor and resistor to pins 5 and 6 controls the TL494 oscillator frequency. The oscillator is set to operate at 20 kHz, using the component values calculated by equations 8 and 9:

$$f_{OSC} = 1/(R_T \times C_T) \quad (8)$$

Choose C_T = 0.001 µF and calculate R_T:

$$R_T = 1/(f_{OSC} \times C_T) = 1/[(20 \times 10^3) \times (0.001 \times 10^{-6})] = 50\ k\Omega \quad (9)$$

Error Amplifier

The error amplifier compares a sample of the 5-V output to the reference and adjusts the PWM to maintain a constant output current (see Figure 36).

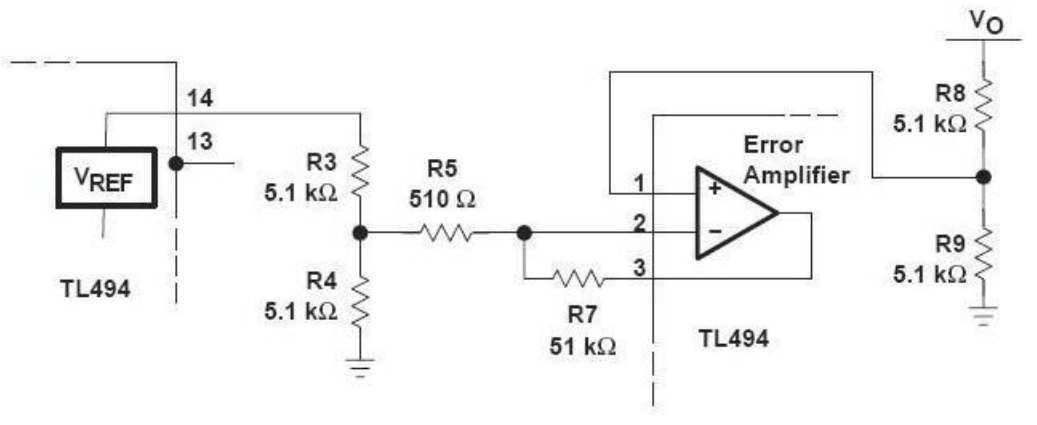


Figure 36. Error-Amplifier Section

The TL494 internal 5-V reference is divided to 2.5 V by R3 and R4. The output-voltage error signal also is divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5.0 V, a 10-kΩ potentiometer can be used in place of R8 to provide an adjustment. To increase the stability of the error-amplifier circuit, the output of the error amplifier is fed back to the inverting input through R7, reducing the gain to 100.

Current-Limiting Amplifier

The power supply was designed for a 10-A load current and an IL swing of 1.5 A; therefore, the short-circuit current should be:

$$I_{SC} = I_O + (I_L/2) = 10.75\ A \qquad (10)$$

The current-limiting circuit is shown in Figure 37.

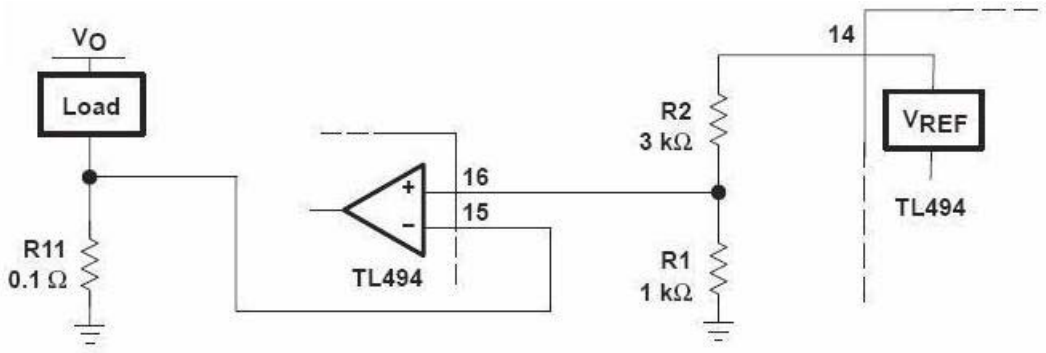


Figure 37. Current-Limiting Circuit

Resistors R1 and R2 set the reference of about 1 V on the inverting input of the current-limiting amplifier. Resistor R11, in series with the load, applies 1 V to the non inverting terminal of the current-limiting amplifier when the load current reaches 10 A. The output-pulse width is reduced accordingly. The value of R11 is:

$$R11 = 1V/10\,A = 0.1\,\Omega \qquad (11)$$

Soft Start and Dead Time

To reduce stress on the switching transistors at start-up, the start-up surge that occurs as the output filter capacitor charges must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit relatively simple (see Figure 38).

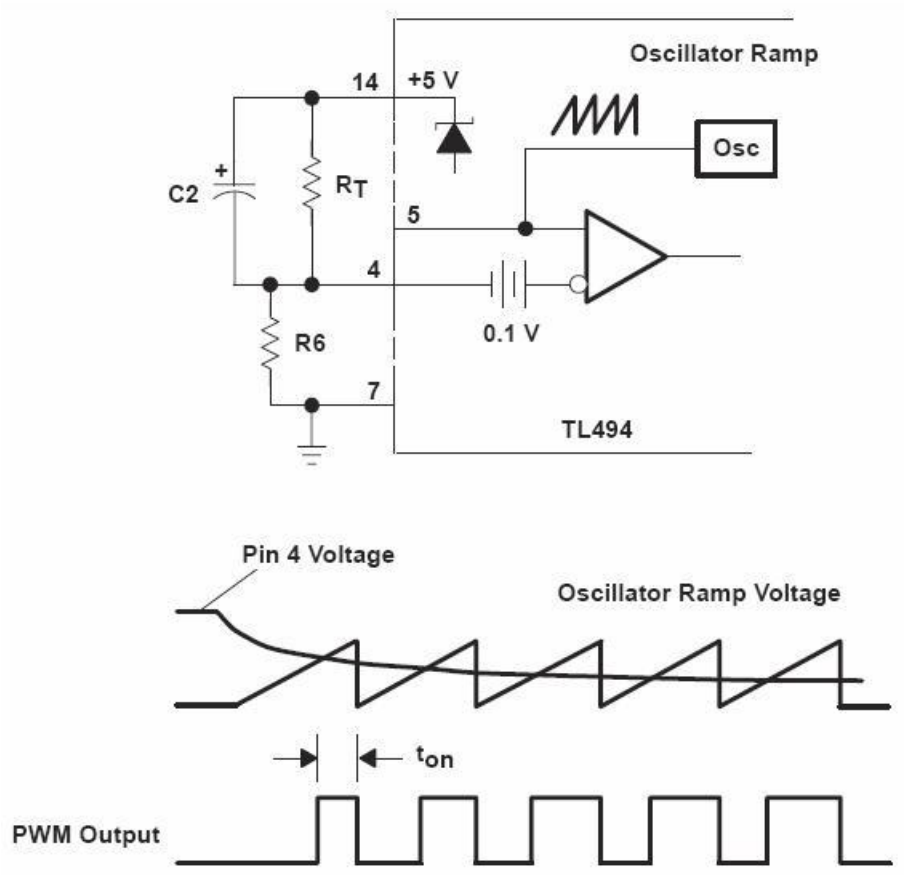


Figure 38. Soft-Start Circuit

The soft-start circuit allows the pulse width at the output to increase slowly (see Figure 38) by applying a negative slope waveform to the dead-time control input (pin 4). Initially, capacitor C2 forces the dead-time control input to follow the 5-V regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output pulse width

slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after start-up is 0.1 × 5 V, or 0.5 V.
The soft-start time generally is in the range of 25 to 100 clock cycles. If 50 clock cycles at a 20-kHz switching rate is selected, the soft-start time is:

$$t = 1/f = 1/20\ kHz = 50\ \mu s\ per\ clock\ cycle \quad (12)$$

The value of the capacitor then is determined by:

$$C2 = soft\text{-}start\ time/R6 = (50\ \mu s \times 50\ cycles)/1\ k\Omega = 2.5\ \mu s \quad (13)$$

This helps eliminate any false signals that might be created by the control circuit as power is applied.

Inductor Calculations

The switching circuit used is shown in Figure 39.

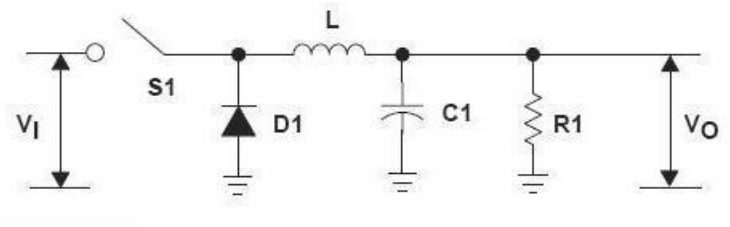


Figure 39. Switching Circuit

The size of the inductor (L) required is:

d = duty cycle = V_O/V_I = 5 V/32 V = 0.156
f = 20 kHz (design objective)
t_{on} = time on (S1 closed) = (1/f) × d = 7.8 µs
t_{off} = time off (S1 open) = (1/f) – t_{on} = 42.2 µs
L $\simeq (V_I - V_O) \times t_{on}/\Delta I_L$
$\simeq$ [(32 V – 5 V) × 7.8 µs]/1.5 A
$\simeq$ 140.4 µH

Output Capacitance Calculations

Once the filter inductor has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important. So, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and the peak-to-peak ripple current.

$$ESR(max) = \Delta V_{O(ripple)}/\Delta I_L = V/1.5\,A = 0.067\,\Omega \qquad (14)$$

The minimum capacitance of C3 necessary to maintain the VO ripple voltage at less than the 100-mV design objective was calculated according to equation 15:

$$C3 = \Delta I_L/\left(8f\Delta V_O\right) = 1.5\,A/\left(8 \times 20 \times 10^3 \times 0.1\,V\right) = 94\,\mu F \qquad (15)$$

A 220-mF, 60-V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8 A.

Transistor Power-Switch Calculations

The transistor power switch was constructed with an NTE153 pnp drive transistor and an NTE331 npn output transistor. These two power devices were connected in a pnp hybrid Darlington circuit configuration (see Figure 40).

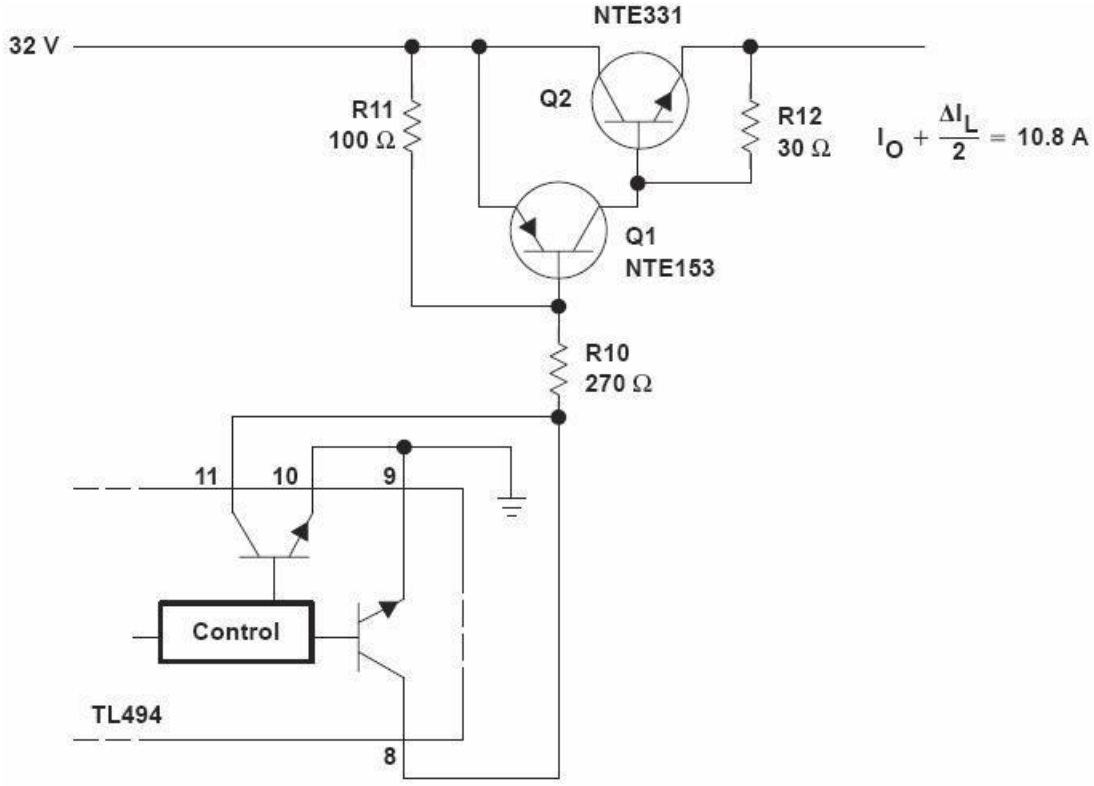


Figure 40. Power-Switch Section

The hybrid Darlington circuit must be saturated at a maximum output current of IO + ΔIL/2 or 10.8 A. The Darlington hfe at 10.8 A must be high enough not to exceed the 250-mA maximum output collector current of the TL494. Based on published NTE153 and NTE331 specifications, the required power-switch minimum drive was calculated by equations 16–18 to be 144 mA:

$$h_{FE}(Q1) \text{ at } I_C \text{ of } 3\ A = 15 \quad (16)$$

$$h_{FE}(Q2) \text{ at } I_C \text{ of } 10.0\ A = 5 \quad (17)$$

$$i_B \geq [I_O + (I_L/2)] / [h_{FE}(Q2) \times h_{FE}(Q1)] \geq 144\ mA \quad (18)$$

The value of R10 was calculated by:

$$R10 \leq \{V_I - [V_{BF}(Q1) + V_{CF}(TL494)]\}/[i_B] = [32 - (1.5 + 0.7)]/(0.144) \quad (19)$$

Based on these calculations, the nearest standard resistor value of 220 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in switching transistors when they are turned off. The power supply described demonstrates the flexibility of the TL494 PWM control circuit. This power-supply design demonstrates many of the power-supply control methods provided by the TL494, as well as the versatility of the control circuit.

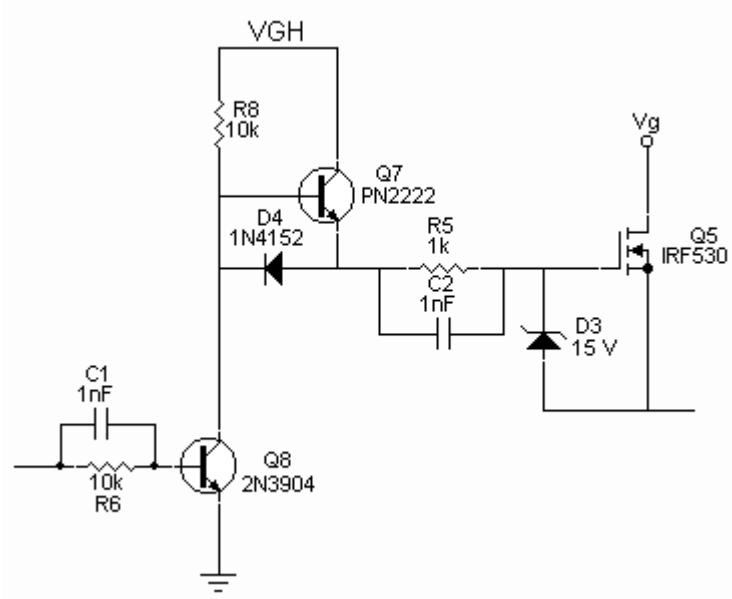
3 UNIDAD 2. Fuentes de alimentación conmutadas.

3.1 Conceptos básicos (2.1)

3.1.1 High-Side Gate Drivers

High-side gate drivers are used to drive a MOSFET or IGBT that is connected to the positive supply and is not ground-referenced but is floating. High-side drivers are more complicated than low-side drivers because of the required voltage translation to the supply and because it is more difficult to turn off a floating transistor.
Gate drivers are available as ICs, such as the IR2112, that drives gates elevated to several hundred volts. A high and low-side driver are provided for about $1.50 in a 14-pin IC. Other suppliers, such as Intersil and Siliconix, also have integrated high-side drivers. These are typically implemented by floating an RS flop off the high-side supply rail and using two ground-referenced (low-side) high-voltage transistors to pulse the R and S inputs. The RS-flop output is buffered by a high-current driver, with bootstrapping circuitry to provide gate-voltage drive (V_{GH}) above the supply rail (V_g). In addition to the basic driver function, short-circuit, undervoltage, and thermal protection functions are sometimes added. Integrated gate drivers are a good alternative in many applications, but if space is not limited, a discrete solution using commodity transistors, diodes, resistors and a capacitor or two can be lower in cost. Consequently, a survey of direct-coupled high-side drivers follows.

3.1.1.1 Inverting Direct-Coupled High-Side Driver

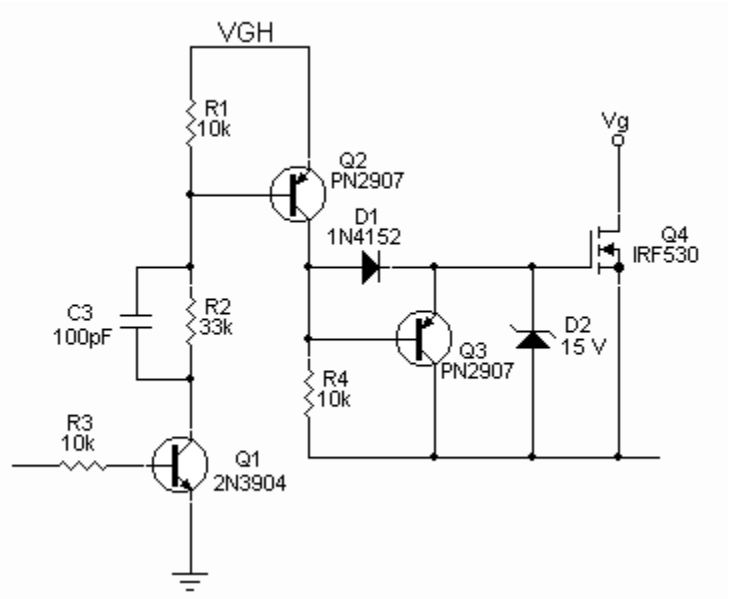


The first direct-coupled circuit is shown below. A logic high level at the input turns MOSFET Q5 off. When Q8 conducts, it pulls its collector voltage to near-zero volts, and the gate capacitance is discharged through D4 and Q8. For motor-drive applications, the induced voltage of the motor can drive the output, causing current to flow through the gate protection Zener, D3, diode D4, and Q8 without current limiting. R5 is added to limit reverse current. If R5 must be made so large that gate drive switching times become too slow, then speed-up capacitor

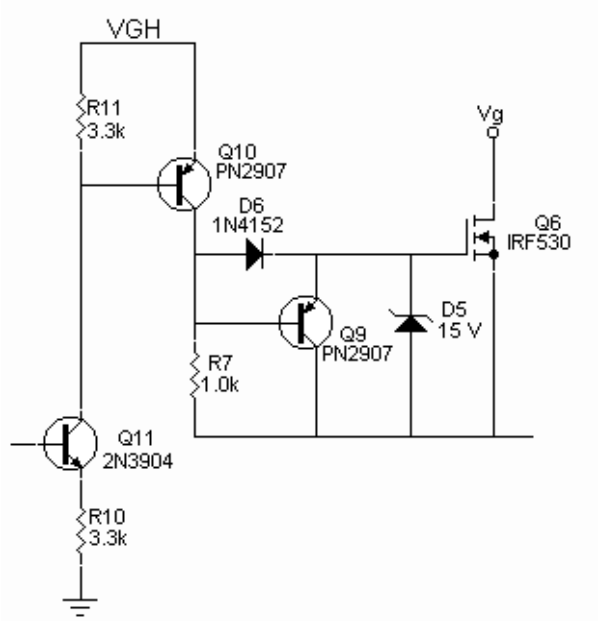
C2 is added. Because Q8 saturates when turned on, C1 speeds up transition times. This particular circuit turns off slowly, but quicker turn-off is easily achieved by reducing the value of R8 at the expense of greater power dissipation when Q8 is on.
This driver has the disadvantage that Q8 must pull down to ground, causing its collector to swing the full supply voltage. This large *dv/dt* causes electrical noise and large parasitic capacitive currents. But it is a discrete minimum-part circuit that can be optimal for drivers operating under 100 V. The parts cost is less that $0.50 (omitting Q5).

3.1.1.2 Noninverting Direct-Coupled High-Side Driver

Another basic driver is shown below. It mainly differs from the previous driver in that it uses an inverting PNP output stage to drive a floating gate. When Q1 turns on, it drives Q2 on, which drives the power MOSFET (Q4) gate. Gate turn-off is accomplished by the floating PNP, Q3, which is driven on (once Q2 is off) by the voltage across the gate-source capacitance, through R4. Diode D1 is off during turn-off. This circuit has an advantage over the inverting driver in that the output circuit driving the gate is floating, isolated by the collector of Q2. Consequently, for motor-drives, no reverse current path from output through Zener D2 exists. At power-on, a conduction path through the collector of Q2 can be thwarted if problematic by placing a diode in series with the Q2 collector.
This particular circuit, when using a supply of 20 V, has a turn-on time of about 1 ms, a turn-off delay of about 2 ms and a turn-off time of about 2 ms, a low-power but excessively slow circuit. A much-improved circuit is shown below.
The biggest improvement is to remove R2, C3 and add R10. The collector current is now determined by R10 and the logic high level applied at the input, to the base of Q11. While on, power that would have been dissipated in R10 transfers to Q11, and for high-voltage applications, R2 and C3 may be included, but at an R2 value that will not saturate Q11. This change decreases switching time significantly.



To decrease turn-off time, R11 is reduced in value to discharge the base of Q10 and turn it off quicker. A smaller R11 does not appreciably increase power dissipation when Q11 is on. Similarly, by decreasing R7, Q9 base current is increased during turn-off, causing Q9 to conduct more current out of the gate, turning it off quicker. A smaller value of R7 will also require greater on-time drive current from Q10, of about V_G(on)/R7. But this is a small fraction of the gate charging current, and R7 can afford to be made relatively small. The improved non-inverting driver has a gate turn-on time of about 400 ns and a comparable turn-off time.
The additional transistor over the inverting driver is more than cost-compensated by elimination of two capacitors and a resistor. Both schemes, with low-side driver (2 BJTs, 2 Rs, 1 D, 1 C) included, cost about $0.40 (1000s), cheap enough to provide a three-phase full-bridge motor driver for the cost of a single half-bridge IC. What compensates somewhat in favor of the IC is the additional board and parts placement cost in assembly. And the added protection functions (which also cost little to implement with discrete parts) must also be taken into account. If you have the space for a discrete solution, it can sometimes be optimal, especially with supplies under 100 V.



3.1.1.3 Closure

The two basic discrete, direct-coupled, high-side drivers are sometimes a preferred alternative to an IC driver, and are cheaper and occupy less board area than transformer-coupled drivers, mainly because of the transformer size and cost. Opto-coupler circuits can also be low in parts count but are somewhat more expensive due to the coupler. While transformers and couplers offer isolation, an isolated (floating) V_{GH} supply may also be required, to swing along with the gate voltage.
Ó *Dennis L. Feucht*, 2001

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3.2 Configuraciones básicas CD-CD y fijas. (2.2)

3.2.1 Understanding Buck Power Stages in Switchmode Power Supplies

Everett Rogers

ABSTRACT
A switching power supply consists of the power stage and the control circuit. The power stage performs the basic power conversion from the input voltage to the output voltage and includes switches and the output filter. This report addresses the buck power stage only and does not cover control circuits. Detailed steady-state and small-signal analysis of the buck power stage operating in continuous and discontinuous mode are presented. Variations in the standard buck power stage and a discussion of power stage component requirements are included.

Contents

3.2.1.1 1 Introduction

The three basic switching power supply topologies in common use are the buck, boost, and buck-boost. These topologies are nonisolated, that is, the input and output voltages share a common ground. There are, however, isolated derivations of these nonisolated topologies. The power supply topology refers to how the switches, output inductor, and output capacitor are connected. Each topology has unique properties. These properties include the steady-state voltage conversion ratios, the nature of the input and output currents, and the character of the output voltage ripple. Another important property is the frequency response of the duty-cycle-to-output-voltage transfer function. The most common and probably the

simplest power stage topology is the buck power stage, sometimes called a step-down power stage. Power supply designers choose the buck power stage because the output voltage is always less than the input voltage in the same polarity and is not isolated from the input. The input current for a buck power stage is discontinuous or pulsating due to the power switch (Q1) current that pulses from zero to IO every switching cycle. The output current for a buck power stage is continuous or nonpulsating because the output current is supplied by the output inductor/capacitor combination; the output capacitor never supplies the entire load current (for continuous inductor current mode operation, one of the two operating modes to be discussed in the next section). This report describes the steady state operation of the buck power stage in continuous-mode and discontinuous-mode operation with ideal waveforms given. The duty-cycle-to-output-voltage transfer function is given after an introduction of the PWM switch model. Figure 1 shows a simplified schematic of the buck power stage with a drive circuit block included. The power switch, Q1, is an n-channel MOSFET. The diode, CR1, is usually called the catch diode, or freewheeling diode. The inductor, L, and capacitor, C, make up the output filter. The capacitor ESR, RC, (equivalent series resistance) and the inductor DC resistance, RL , are included in the analysis. The resistor, R, represents the load seen by the power stage output.

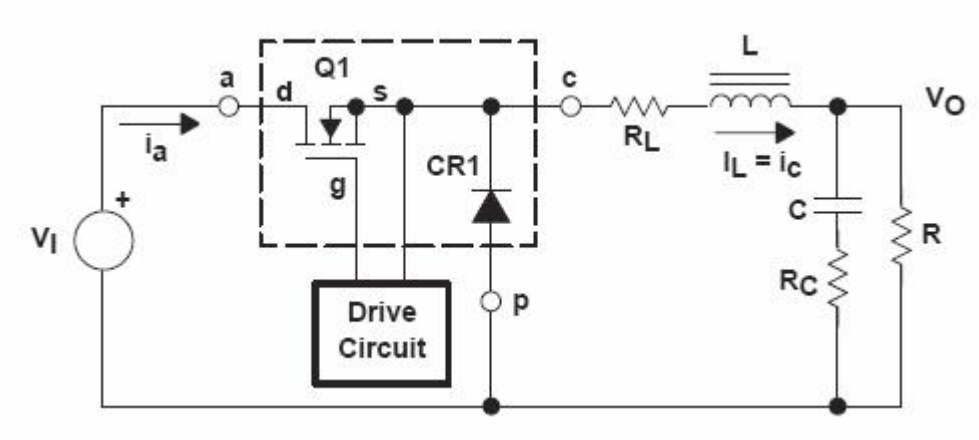

Figure 1. Buck Power Stage Schematic

During normal operation of the buck power stage, Q1 is repeatedly switched on and off with the on and off times governed by the control circuit. This switching action causes a train of pulses at the junction of Q1, CR1, and L which is filtered by the L/C output filter to produce a dc output voltage, VO. A more detailed quantitative analysis is given in the following sections.

3.2.1.2 2 Buck Power Stage Steady-State Analysis

A power stage can operate in continuous or discontinuous inductor current mode. Continuous inductor current mode is characterized by current flowing continuously in the inductor during the entire switching cycle in steady state operation. Discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. The two different modes are discussed in greater detail later and design guidelines for the inductor value to maintain a chosen mode of operation as a function of rated load is given. It is very

desirable for a power stage to stay in only one mode over its expected operating conditions, because the power stage frequency response changes significantly between the two modes of operation.
For this analysis, an n-channel power MOSFET is used and a positive voltage, VGS(ON) , is applied from the Gate to the Source terminals of Q1 by the drive circuit to turn ON the FET. The advantage of using an n-channel FET is its lower RDS(on) but the drive circuit is more complicated because a floating drive is required. For the same die size, a p-channel FET has a higher RDS(on) but usually does not require a floating drive circuit. The transistor Q1 and diode CR1 are drawn inside a dashed-line box with terminals labeled a, p, and c. The inductor current IL is also labeled iC and refers to current flowing out of terminal c. These items are explained fully in the Buck Power Stage Modeling section.

3.2.1.2.1 2.1 Buck Steady-State Continuous Conduction Mode Analysis

The following is a description of steady-state operation in continuous conduction mode. The main result of this section is a derivation of the voltage conversion relationship for the continuous conduction mode buck power stage. This result is important because it shows how the output voltage depends on duty cycle and input voltage or, conversely, how the duty cycle can be calculated based on input voltage and output voltage. Steady-state implies that the input voltage, output voltage, output load current, and duty-cycle are fixed and not varying. Capital letters are generally given to variable names to indicate a steady-state quantity. In continuous conduction mode, the Buck power stage assumes two states per switching cycle. The ON state is when Q1 is ON and CR1 is OFF. The OFF state is when Q1 is OFF and CR1 is ON. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuits during each state. The circuit diagram for each of the two states is shown in Figure 2.

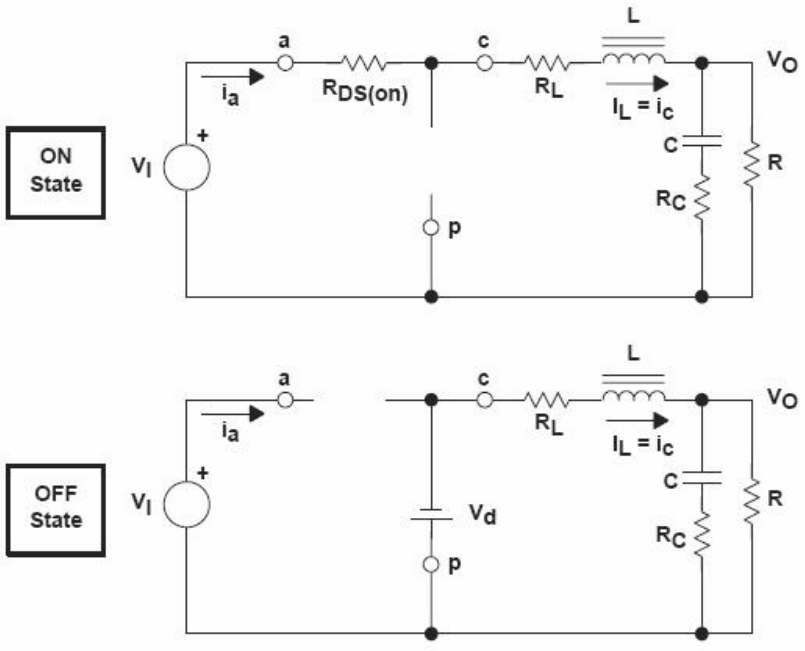

Figure 2. Buck Power Stage States

The duration of the ON state is D × TS = TON where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, Ts . The duration of the OFF state is called TOFF. Since there are only two states per switching cycle for continuous mode, TOFF is equal to (1–D) × TS . The quantity (1–D) is sometimes called D4. These times are shown along with the waveforms in Figure 3.

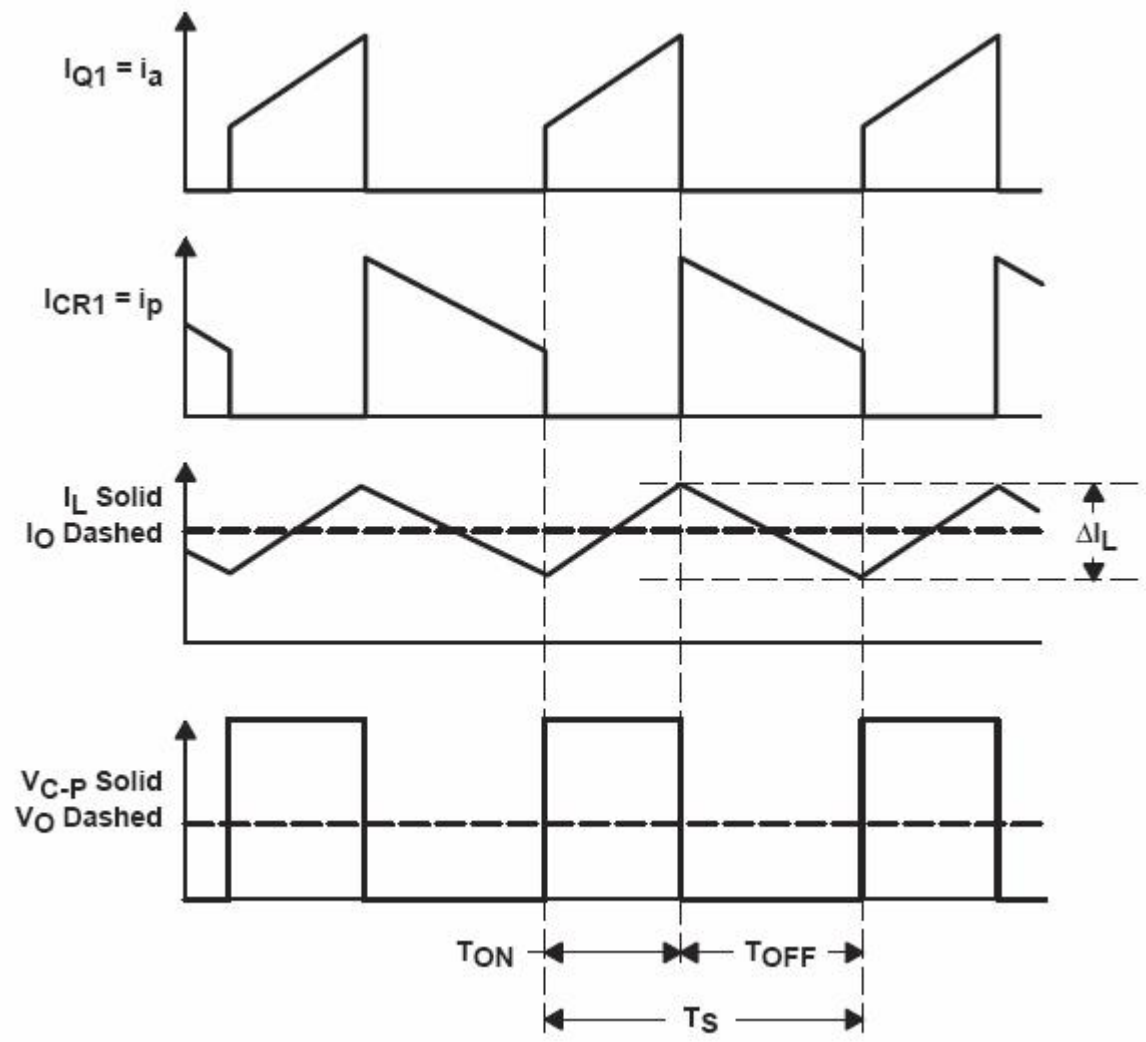

Figure 3. Continuous-Mode Buck Power Stage Waveforms

Referring to Figure 2, during the ON state, Q1 presents a low resistance, RDS(on) , from its drain to source and has a small voltage drop of VDS = IL × RDS(on) . There is also a small voltage drop across the dc resistance of the inductor equal to IL × RL . Thus, the input voltage, VI , minus losses, (VDS + IL × RL), is applied to the left-hand side of inductor, L. CR1 is OFF during this time because it is reverse biased. The voltage applied to the right hand side of L is simply the output voltage, VO. The inductor current, IL , flows from the input source, VI , through Q1 and to the output capacitor and load resistor combination. During the ON state, the voltage applied across the inductor is constant and equal to VI –

VDS – IL × RL – Vo. Adopting the polarity convention for the current IL shown in Figure 2, the inductor current increases as a result of the applied voltage. Also, since the applied voltage is essentially constant, the inductor current increases linearly. This increase in inductor current during TON is illustrated in Figure 3. The amount that the inductor current increases can be calculated by using a version of the familiar relationship:

$$V_L = L \times \frac{di_L}{dt} \Rightarrow \Delta I_L = \frac{V_L}{L} \times \Delta T$$

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{\left(V_I - V_{DS} - I_L \times R_L\right) - V_O}{L} \times T_{ON}$$

This quantity, DIL(+), is referred to as the inductor ripple current.

Referring to Figure 2, when Q1 is OFF, it presents a high impedance from its drain to source. Therefore, since the current flowing in the inductor L cannot change instantaneously, the current shifts from Q1 to CR1. Due to the decreasing inductor current, the voltage across the inductor reverses polarity until rectifier CR1 becomes forward biased and turns ON. The voltage on the left-hand side of L becomes –(Vd + IL × RL) where the quantity, Vd , is the forward voltage drop of CR1. The voltage applied to the right hand side of L is still the output voltage, VO. The inductor current, IL , now flows from ground through CR1 and to the output capacitor and load resistor combination. During the OFF state, the magnitude of the voltage applied across the inductor is constant and equal to (VO + Vd + IL × RL). Maintaining our same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the ON time). Hence, the inductor current decreases during the OFF time. Also, since the applied voltage is essentially constant, the inductor current decreases linearly. This decrease in inductor current during TOFF is illustrated in Figure 3.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{V_O + \left(V_d + I_L \times R_L\right)}{L} \times T_{OFF}$$

This quantity, DIL(–), is also referred to as the inductor ripple current.

In steady state conditions, the current increase, DIL(+), during the ON time and the current decrease during the OFF time, DIL(–), must be equal. Otherwise, the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. Therefore, these two equations can be equated and solved for VO to obtain the continuous conduction mode buck voltage conversion relationship.

Solving for VO:

$$V_O = \left(V_I - V_{DS}\right) \times \frac{T_{ON}}{T_{ON} + T_{OFF}} - V_d \times \frac{T_{OFF}}{T_{ON} + T_{OFF}} - I_L \times R_L$$

And, substituting TS for TON + TOFF, and using D = TON/TS and (1–D) = TOFF/TS, the steady-state equation for VO is:

$$V_O = \left(V_I - V_{DS}\right) \times D - V_d \times (1-D) - I_L \times R_L$$

Notice that in simplifying the above, TON + TOFF is assumed to be equal to TS. This is true only for continuous conduction mode as we will see in the discontinuous conduction mode analysis.

NOTE: An important observation should be made here: Setting the two values of DIL equal to each other is equivalent to balancing the volt-seconds on the inductor. The volt-seconds applied to the inductor is the product of the voltage applied and the time that the voltage is applied. This is the best way to calculate unknown values such as VO or D in terms of known circuit parameters and this method will be applied repeatedly in this paper. Volt-second balance on the inductor is a physical necessity and should be comprehended at least as well as Ohms Law.

In the above equations for DIL(+) and DIL(–), the dc output voltage was implicitly assumed to be constant with no AC ripple voltage during the ON time and the OFF time. This is a common simplification and involves two separate effects. First, the output capacitor is assumed to be large enough that its voltage change is negligible. Second, the voltage across the capacitor ESR is also assumed to be negligible. These assumptions are valid because the ac ripple voltage is designed to be much less than the dc part of the output voltage. The above voltage conversion relationship for VO illustrates the fact that VO can be adjusted by adjusting the duty cycle, D, and is always less than the input because D is a number between 0 and 1. A common simplification is to assume VDS, Vd , and RL are small enough to ignore. Setting VDS, Vd , and RL to zero, the above equation simplifies considerably to:

$$V_O = V_I \times D$$

Another simplified way to visualize the circuit operation is to consider the output filter as an averaging network. This is a valid simplification because the filter cutoff frequency (usually between 500 Hz and 5 kHz) is always much less than the power supply switching frequency (usually between 100 kHz and 500 kHz). The input voltage applied to the filter is the voltage at the junction of Q1, CR1, and L, labeled as Vc–p . The filter passes the dc component (or average) of Vc–p and greatly attenuates all frequencies above the output filter cutoff frequency. Thus, the output voltage is simply the average of the Vc–p voltage. To relate the inductor current to the output current, referring to Figures 2 and 3, note that the inductor delivers current to the output capacitor and load resistor combination during the whole switching cycle. The inductor current averaged over the switching cycle is equal to the output current. This is true because the average current in the output capacitor must be zero. In equation form, we have:

$$I_{L(Avg)} = I_O$$

This analysis was for the buck power stage operation in continuous inductor current mode. The next section is a description of steady-state operation in discontinuous conduction mode. The main result is a derivation of the voltage conversion relationship for the discontinuous conduction mode buck power stage

3.2.1.2.2 2.2 Buck Steady-State Discontinuous Conduction Mode Analysis

We now investigate what happens when the load current is decreased. First, observe that the power stage output current is the average of the inductor current.

This should be obvious since the inductor current flows into the output capacitor and load resistor combination and the average current flowing in the output capacitor is always zero.

If the output load current is reduced below the critical current level, the inductor current will be zero for a portion of the switching cycle. This should be evident from the waveforms shown in Figure 3 since the peak to peak amplitude of the ripple current does not change with output load current. In a (non synchronous) buck power stage, if the inductor current attempts to fall below zero, it just stops at zero (due to the unidirectional current flow in CR1) and remains there until the beginning of the next switching cycle. This operating mode is called discontinuous conduction mode. A power stage operating in discontinuous conduction mode has three unique states during each switching cycle as opposed to two states for continuous conduction mode. The load current condition where the power stage is at the boundary between continuous and discontinuous mode is shown in Figure 4. This is where the inductor current falls to zero and the next switching cycle begins immediately after the current reaches zero.

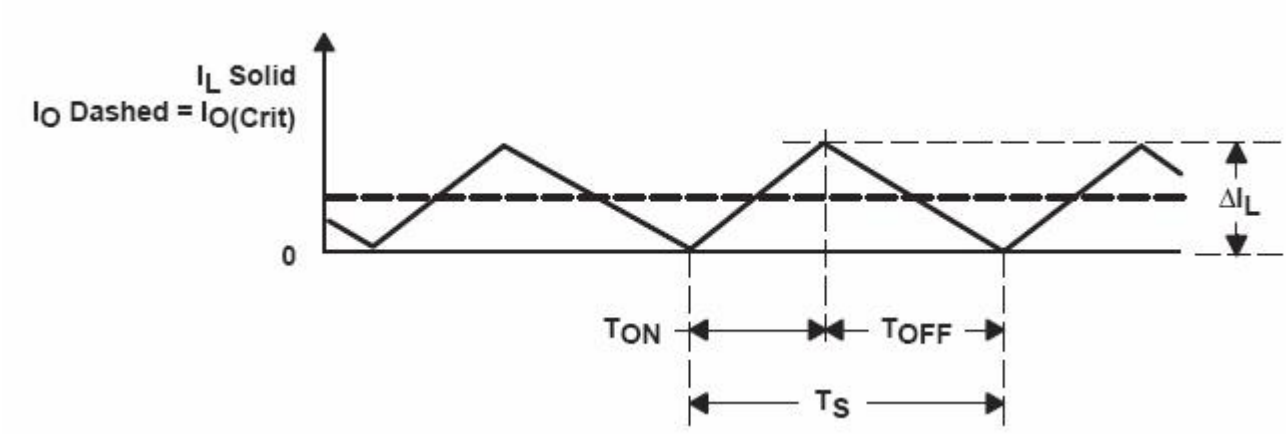

Figure 4. Boundary Between Continuous and Discontinuous Mode

Further reduction in output load current puts the power stage into discontinuous conduction mode. This condition is illustrated in Figure 5. The discontinuous mode power stage frequency response is quite different from the continuous mode frequency response and is shown in the Buck Power Stage Modeling section. Also, the input to output relationship is quite different as shown in the following derivation.

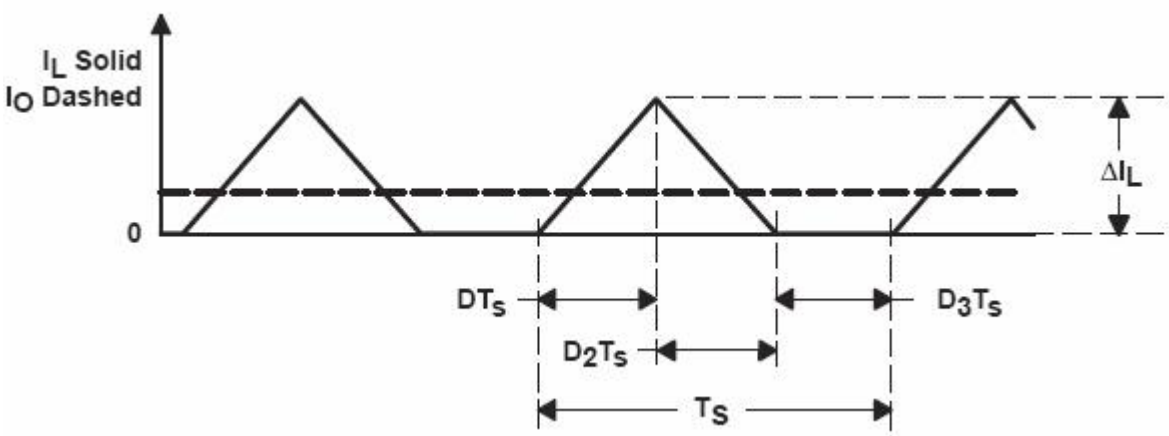

Figure 5. Discontinuous Current Mode

To begin the derivation of the discontinuous conduction mode buck power stage voltage conversion ratio, observe that there are three unique states that the power stage assumes during discontinuous current mode operation. The ON state is when Q1 is ON and CR1 is OFF. The OFF state is when Q1 is OFF and CR1 is ON. The IDLE state is when both Q1 and CR1 are OFF. The first two states are identical to those of the continuous mode case and the circuits of Figure 2 are applicable except that TOFF p (1–D) × TS. The remainder of the switching cycle is the IDLE state. In addition, the dc resistance of the output inductor, the output diode forward voltage drop, and the power MOSFET ON-state voltage drop are all

assumed to be small enough to omit. The duration of the ON state is TON = D × TS where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, Ts . The duration of the OFF state is TOFF = D2 × TS. The IDLE time is the remainder of the switching cycle and is given as TS – TON – TOFF = D3 × TS. These times are shown with the waveforms in Figure 6. Without going through the detailed explanation as before, the equations for the inductor current increase and decrease are given below. The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{V_I - V_O}{L} \times T_{ON} = \frac{V_I - V_O}{L} \times D \times T_S = I_{PK}$$

The ripple current magnitude, DIL(+), is also the peak inductor current, Ipk , because in discontinuous mode, the current starts at zero each cycle. The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{V_O}{L} \times T_{OFF}$$

As in the continuous conduction mode case, the current increase, DIL(+), during the ON time and the current decrease during the OFF time, DIL(–), are equal. Therefore, these two equations can be equated and solved for VO to obtain the first of two equations to be used to solve for the voltage conversion ratio:

$$V_O = V_I \times \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_I \times \frac{D}{D + D2}$$

Now we calculate the output current (the output voltage VO divided by the output load R). It is the average of the inductor current.

$$I_O = I_{L(avg)} = \frac{V_O}{R} = \frac{I_{PK}}{2} \times \frac{D \times T_S + D2 \times T_S}{Ts}$$

Now, substitute the relationship for IPK into the above equation to obtain:

$$I_O = \frac{V_O}{R} = \left(V_I - V_O\right) \times \frac{D \times T_S}{2 \times L} \times (D + D2)$$

We now have two equations, the one for the output current just derived and the one for the output voltage (above), both in terms of VI , D, and D2. We now solve each equation for D2 and set the two equations equal to each other. Using the resulting equation, an expression for the output voltage, VO, can be derived.
The discontinuous conduction mode buck voltage conversion relationship is given by:

$$V_O = V_I \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

The above relationship shows one of the major differences between the two conduction modes. For discontinuous conduction mode, the voltage conversion relationship is a function of the input voltage, duty cycle, power stage inductance, the switching frequency and the output load resistance while for continuous conduction mode, the voltage conversion relationship is only dependent on the input voltage and duty cycle.

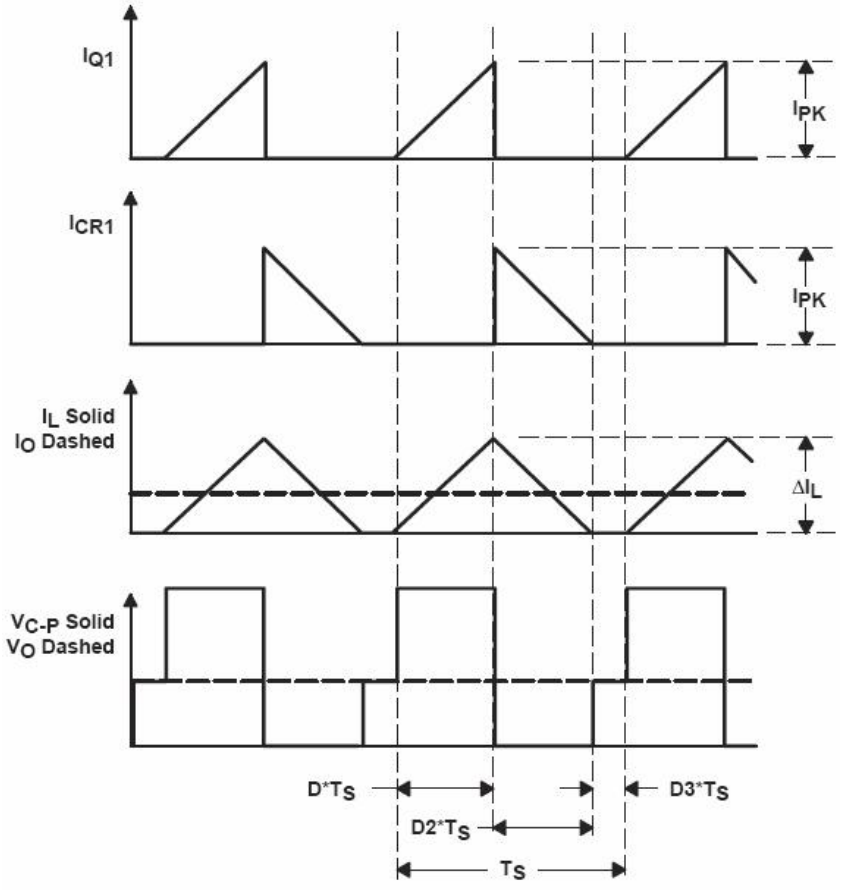

Figure 6. Discontinuous-Mode Buck Power Stage Waveforms

It should be noted that the buck power stage is rarely operated in discontinuous conduction mode in normal situations, but discontinuous conduction mode will occur anytime the load current is below the critical level.

3.2.1.2.3 2.3 Critical Inductance

The previous analyses for the buck power stage have been for continuous and discontinuous conduction modes of steady-state operation. The conduction mode of a power stage is a function of input voltage, output voltage, output current, and the value of the inductor. A buck power stage can be designed to operate in continuous mode for load currents above a certain level usually 5% to 10% of full load. Usually, the input voltage range, the output voltage and load current are defined by the power stage specification. This leaves the inductor value as the design parameter to maintain continuous conduction mode.

The minimum value of inductor to maintain continuous conduction mode can be determined by the following procedure.
First, define IO(crit) as the minimum current to maintain continuous conduction mode, normally referred to as the critical current. This value is shown in Figure 4 and is calculated as:

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$$I_{O(crit)} = \frac{\Delta I_L}{2}$$

Second, calculate L such that the above relationship is satisfied. To solve the above equation, either relationship, DIL(+) or DIL(–) may be used for DIL . Note also that either relationship for DIL is independent of the output current level. Here, DIL(–) is used. The worst case condition (giving the largest Lmin) is at maximum input voltage because this gives the maximum DIL . Now, substituting and solving for Lmin :

$$L_{min} \geq \frac{1}{2} \times \left(V_O + V_d + I_L \times R_L\right) \times \frac{T_{OFF(max)}}{I_{O(crit)}}$$

The above equation can be simplified and put in a form that is easier to apply as shown:

$$L_{min} \geq \frac{V_O \times \left[1 - \frac{V_O}{V_{I(max)}}\right] \times T_S}{2 \times I_{O(crit)}}$$

Using the inductor value just calculated will guarantee continuous conduction mode operation for output load currents above the critical current level, IO(crit) .

3.2.1.3 3 Buck Power Stage Small Signal Modeling

We now switch gears moving from a detailed circuit oriented analysis approach to more of a system level investigation of the buck power stage. This section presents techniques to assist the power supply designer in accurately modelling the power stage as a component of the control loop of a buck power supply. The three major components of the power supply control loop (i.e., the power stage, the pulse width modulator and the error amplifier) are shown in block diagram form in Figure 7.

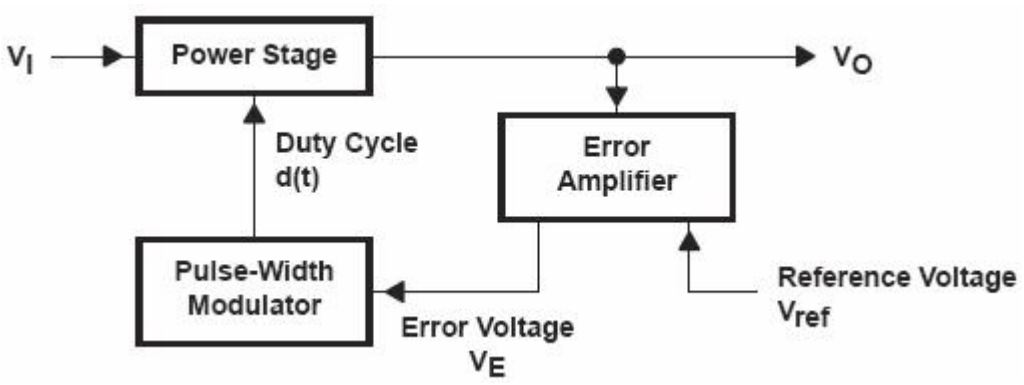

Figure 7. Power Supply Control Loop Components

Modeling the power stage presents one of the main challenges to the power supply designer. A popular technique involves modeling only the switching elements of the power stage. An equivalent circuit for these elements is derived and is called the PWM Switch Model where PWM is the abbreviation for pulse width modulated. This approach is presented here.
As shown in Figure 7, the power stage has two inputs: the input voltage and the duty cycle. The duty cycle is the control input, i.e., this input is a logic signal which controls the switching action of the power stage and hence the output voltage.
Even though the buck power stage has an essentially linear voltage conversion ratio versus duty cycle, many other power stages have a nonlinear voltage conversion ratio versus duty cycle. To illustrate this nonlinearity, a graph of the steady-state voltage conversion ratio for a boost power stage as a function of steady-state duty cycle, D is shown in Figure 8. The nonlinear boost power stage is used here for illustration to stress the significance of deriving a linear model.
The nonlinear characteristics are a result of the switching action of the power stage switching components, Q1 and CR1. It was observed in reference [5] that the only nonlinear components in a power stage are the switching devices; the remainder of the circuit consists of linear elements. It was also shown in reference [5] that a linear model of only the nonlinear components could be derived by averaging the voltages and currents associated with these nonlinear components over one switching cycle. The model is then substituted into the original circuit for analysis of the complete power stage. Thus, a model of the switching devices is given and is called the PWM switch model.

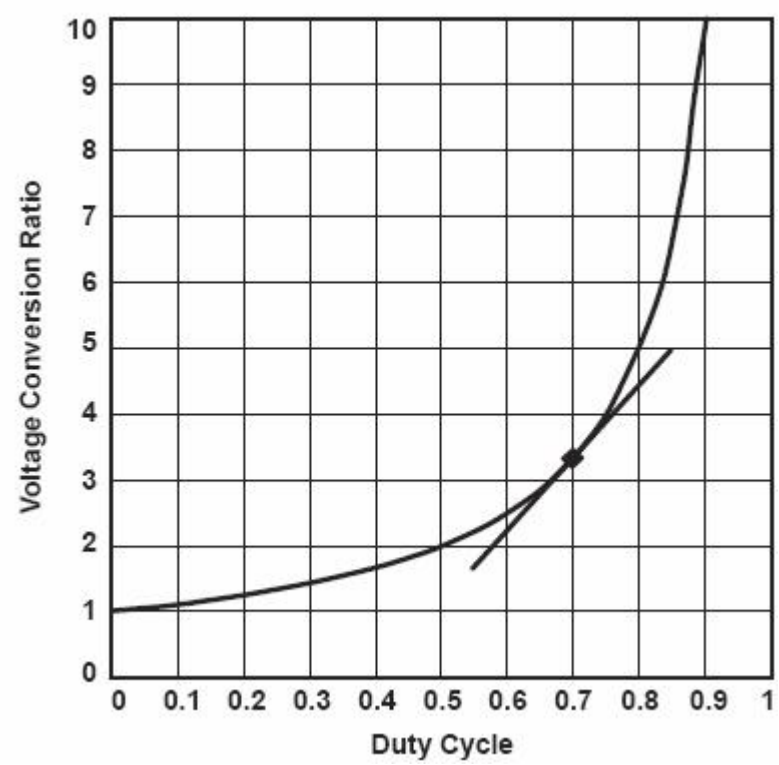

Figure 8. Boost Nonlinear Power Stage Gain vs Duty Cycle

The basic objective behind modelling power stages is to represent the ac behavior at a given operating point and to be linear around the operating point.
We want linearity so that we can apply the many analysis tools available for linear systems. Referring again to Figure 8, if we choose the operating point at D = 0.7, a straight line can be constructed that is tangent to the original curve at the point where D = 0.7. This is an illustration of linearization about an operating point, a technique used in deriving the PWM switch model. Qualitatively, one can see that if the variations in duty cycle are kept small, a linear model accurately represents the nonlinear behavior of the power stage being analyzed.

Since a power stage can operate in one of two conduction modes, i.e., continuous conduction mode (CCM) or discontinuous conduction mode (DCM), there is a PWM switch model for the two conduction modes. The CCM PWM Switch model is derived here. The DCM PWM switch model is derived in the Application Report Understanding Buck–Boost Converter Power Stages, TI Literature Number SLVA059.

3.2.1.3.1 3.1 Buck Continuous Conduction Mode Small Signal Analysis

To start modeling the buck power stage, we begin with the derivation of the PWM Switch model in (CCM). We focus on the CCM Buck power stage shown in Figure 1. The strategy is to average the switching waveforms over one switching cycle and produce an equivalent circuit for substitution into the remainder of the power stage. The waveforms that are averaged are the voltage across CR1, vc–p , and the current in Q1, ia . The waveforms are shown in Figure 3. Referring again to Figure 1, the power transistor, Q1, and the catch diode,

CR1, are drawn inside a dashed-line box. These are the components that will be replaced by the PWM switch equivalent circuit. The terminals labeled a, p, and c will be used for terminal labels of the PWM switch model.

Now, an explanation of the terminal naming convention is in order. The terminal named a is for active; it is the terminal connected to the active switch. Similarly, p is for passive and is the terminal of the passive switch. Lastly, c is for common and is the terminal that is common to both the active and passive switches.
Interestingly enough, all three commonly used power stage topologies contain active and passive switches and the above terminal definitions can be also applied. In addition, it is true that substituting the PWM switch model that we will derive into other power stage topologies also produces a valid model for that particular power stage. To use the PWM switch model in other power stages, just substitute the model shown below in Figure 10 into the power stage in the appropriate orientation.
Referring to the waveforms in Figure 3, regarded as instantaneous functions of time, the following relationships are true:

$$i_a(t) = \begin{cases} i_c(t) & \text{during } d \times T_S \\ 0 & \text{during } d' \times T_S \end{cases}$$

$$v_{cp}(t) = \begin{cases} v_{ap}(t) & \text{during } d \times T_S \\ 0 & \text{during } d' \times T_S \end{cases}$$

where: ia(t) and ic(t) are the instantaneous currents during a switching cycle and vcp(t) and vap(t) are the instantaneous voltages between the indicated terminals. If we take the average over one switching cycle of the above quantities, we get:

$$\langle i_a \rangle = d \times \langle i_c \rangle \quad (1)$$

$$\langle v_{cp} \rangle = d \times \langle v_{ap} \rangle \quad (2)$$

where the brackets indicate averaged quantities.

Now, we can implement the above averaged equations in a simple circuit using dependent sources:

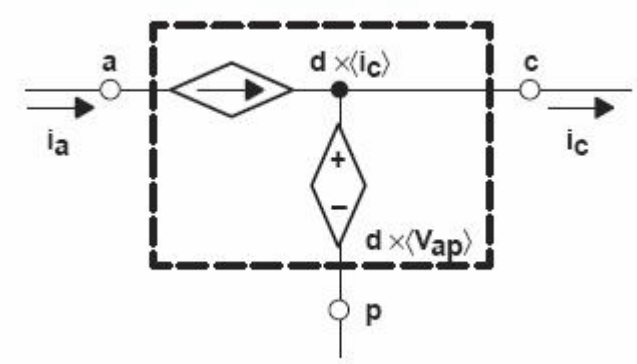

Figure 9. Averaged (Nonlinear) CCM PWM Switch Model

The above model is one form of the PWM switch model. However, in this form it is a large signal nonlinear model. We now need to perform perturbation and linearization and then the PWM switch model will be in the desired form, i.e., linearized about a given operating point.

The main idea of perturbation and linearization is assuming an operating point and introducing small variations about that operating point. For example, we assume that the duty ratio is fixed at d = D (capital letters indicate steady-state, or dc quantities while lower case letters are for time-varying quantities). Then a small variation, d ^ , is added to the duty cycle so that the complete expression for the duty cycle becomes:

$$d(t) = D + \hat{d}(t)$$

Note that the ^ (hat) above the quantities represents perturbed or small ac quantities. We change notation slightly replacing the averaged quantities such as (ia) with capitol letters (indicating dc quantities) such as Ia . Now we apply the above process to equations (1) and (2) to obtain:

$$I_a + \hat{i}_a = \left(D + \hat{d}\right) \times \left(I_c + \hat{i}_c\right) = D \times I_c + D \times \hat{i}_c + \hat{d} \times I_c + \hat{d} \times \hat{i}_c$$

$$V_{cp} + \hat{v}_{cp} = \left(D + \hat{d}\right) \times \left(V_{ap} + \hat{v}_{ap}\right) = D \times V_{ap} + D \times \hat{v}_{ap} + \hat{d} \times V_{ap} + \hat{d} \times \hat{v}_{ap}$$

Now, separate steady-state quantities from ac quantities and also drop products of ac quantities because the variations are assumed to be small and products of two small quantities are assumed to be negligible. We arrive at the steady-state and ac relationships or, in other words, the dc and small signal model:

$$I_a = D \times I_c \qquad \text{Steady-state}$$

$$\hat{i}_a = D \times \hat{i}_c + \hat{d} \times I_c \qquad \text{AC}$$

$$V_{cp} = D \times V_{ap} \qquad \text{Steady-state}$$

$$\hat{v}_{cp} = D \times \hat{v}_{ap} + \hat{d} \times V_{ap} \qquad \text{AC}$$

In order to implement the above equations into a simple circuit, first notice that the two steady-state relationships can be represented by an ideal (independent of frequency) transformer with turns ratio equal to D. Including the ac quantities is straightforward after reflecting all dependent sources to the primary side of the ideal transformer. The dc and small-signal model of the PWM switch is shown in Figure 10. It can easily be verified that the model below satisfies the above four equations.

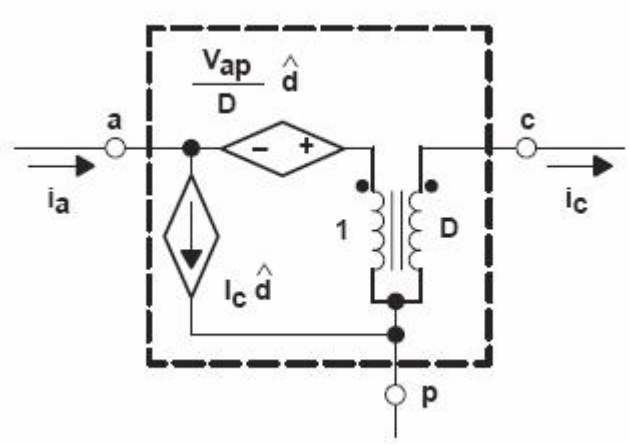

Figure 10. DC and Small Signal CCM PWM Switch Model

This model can now be substituted for Q1 and CR1 in the buck power stage to obtain a model suitable for dc or ac analysis and is shown in Figure 11.

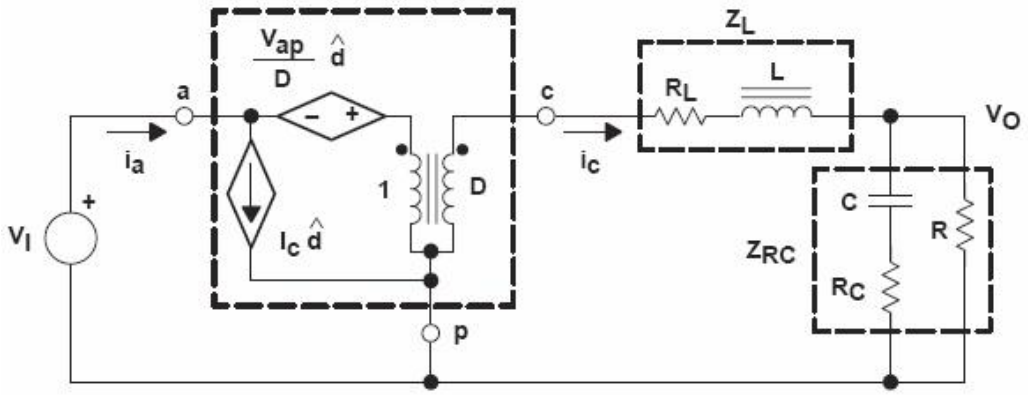

Figure 11. CCM Buck Power Stage Model

To illustrate how simple power stage analysis becomes with the PWM switch model, consider the following. For dc analysis, d ^ is zero, L is a short, and C is an open. Then by inspection one can see VI × D = VO. We also see that Vap = VI .
Thus, knowing the input voltage and output voltage, D is easily calculated. For ac analysis, the following transfer functions can be calculated: open-loop line-to-output, open-loop input impedance, open-loop output impedance, and open-loop control-to-output. The control-to-output, or duty-cycle-to-output, is the transfer function most used for control loop analysis. To determine this transfer function, first, use the results from the DC analysis for operating point information.
This information is used to determine the parameter values of the dependent sources; for example, Vap = VI . Then set the input voltage equal to zero because we only want the ac component of the transfer function. Now, writing a voltage loop equation for the VI – dependent voltage source – transformer primary loop gives the transfer function from duty–cycle to vcp as shown:

$$-\frac{V_{ap}}{D}\times\hat{d}+\frac{\hat{v}_{cp}}{D}=0\Rightarrow\hat{v}_{cp}=V_{ap}\times\hat{d}\Rightarrow\hat{v}_{cp}=V_I\times\hat{d}$$

or

$$\frac{\hat{v}_{cp}}{\hat{d}}=V_I$$

The transfer function from vcp to the output voltage is:

$$\frac{\hat{v}_O}{\hat{v}_{cp}}=\frac{Z_{RC}(s)}{Z_{RC}(s)+Z_L(s)}$$ By voltage division

Where

$$Z_{RC}(s)=\frac{R\times\left(1+s\times R_C\times C\right)}{1+s\times C\times\left(R+R_C\right)}$$ (parallel combination of output R and output C)

$$Z_L(s)=R_L+s\times L$$

So, after simplifying, the duty-cycle-to-output transfer function is:

$$\frac{\hat{v}_O}{\hat{d}}(s) = \frac{\hat{v}_{cp}}{\hat{d}}(s) \times \frac{\hat{v}_O}{\hat{v}_{cp}}(s) = V_I \times \frac{R}{R + R_L} \times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

The above is exactly what is obtained by other modeling procedures.

3.2.1.3.2 3.2 Buck Discontinuous Conduction Mode Small-Signal Analysis

To model the buck power stage operation in discontinuous conduction mode (DCM), we follow a similar path as above for CCM. A PWM switch model is inserted into the power stage circuit by replacing the switching elements. As mentioned above, the derivation for the DCM PWM switch model is given elsewhere. More details can be found in Fundamentals of Power Electronics. The large signal nonlinear version of the DCM PWM switch model is shown in Figure 12. This model is useful for determining the dc operating point of a power supply. The input port is simply modeled with a resistor, Re . The value of Re is given by:

$$R_e = \frac{2 \times L}{D^2 \times T_s}$$

The output port is modeled as a dependent power source. This power source delivers power equal to that dissipated by the input resistor, Re . This model is analogous to the (nonlinear) CCM PWM switch model shown in Figure 9.

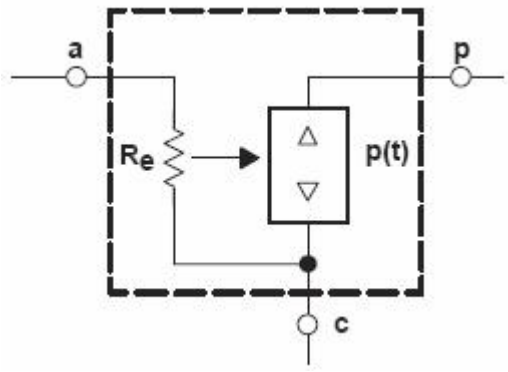

Figure 12. Averaged (Nonlinear) DCM PWM Switch Model

To illustrate discontinuous conduction mode power supply analysis using this model, we examine the buck power stage. The analysis proceeds like the CCM case. The equivalent circuit is substituted into the original circuit. The DCM buck power stage model schematic is shown in the Figure 13.

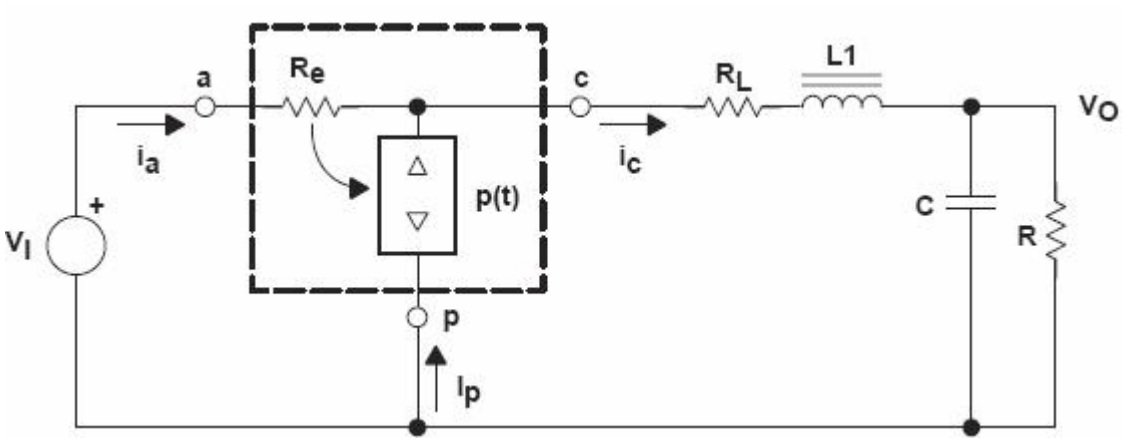

Figure 13. DCM Buck Power Stage DC Model

Notice that this model has the inductor dc resistance included. To illustrate using the model to determine the dc operating point, simply write the equations for the above circuit. This circuit can be described by the network equations shown. First, set the power dissipated in Re equal to the power delivered by the dependent power source:

$$\frac{(V_I - V_{cp})^2}{R_e} = V_{cp} \times I_p$$

Where the current Ip is the difference between IC and IA as follows:

$$I_p = I_c - I_a = \frac{V_O}{R} - \frac{V_I - V_{cp}}{R_e}$$

Now, substitute the equation for Ip into the following equation:

$$\frac{(V_I - V_{cp})^2}{R_e} = V_{cp} \times \left(\frac{V_O}{R} - \frac{V_I - V_{cp}}{R_e} \right)$$

Now we relate VCP to VO as follows:

$$V_{cp} = V_O + \left(\frac{V_O}{R}\right) \times R_L$$

The two equations above can be solved to give VO in terms of VI and D by eliminating Vcp from the two equations and using our previous relationships for Re and K.
The voltage conversion relationship for the DCM buck is given by:

$$V_O = V_I \times \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2} \times \frac{R}{R + R_L}}}$$

This is similar to our previous steady-state result but with the effects of the inductor resistance included.

To derive the small signal model, the circuit of Figure 13 is perturbed and linearized following a procedure similar to the CCM derivation. To see the details of the derivation, the reader is directed to reference [4] for details. The resulting small signal model for the buck power stage operating in DCM is shown in Figure 14.

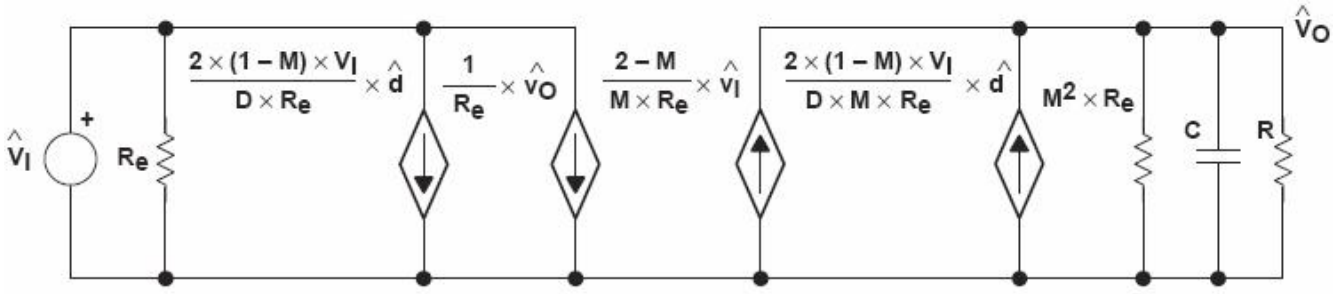

Figure 14. Small Signal DCM PWM Switch Model

The duty-cycle-to-output transfer function for the buck power stage operating in DCM is given by:

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where

$$G_{do} = \frac{2 \times V_O}{D} \times \frac{1 - M}{2 - M}$$

$$D = M \times \sqrt{\frac{K}{1 - M}}$$

$$M = \frac{V_O}{V_I}$$

$$K = \frac{2 \times L}{R \times T_s}$$

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and

$$\omega_p = \frac{2 - M}{1 - M} \times \frac{1}{R \times C}$$

3.2.1.4 4 Variations of the Buck Power Stage

3.2.1.4.1 4.1 Synchronous-Buck Power Stage

A variation of the traditional buck power stage is the synchronous buck power stage. In this power stage, an active switch such as another power MOSFET, Q2 in this example, replaces the rectifier, CR1. The FET is then selected so that its ON-voltage drop is less than the forward drop of the rectifier, thus increasing efficiency. Although this complicates the drive circuit design, the gain in efficiency often makes this an attractive option. Other considerations unique to the synchronous buck power stage are preventing cross–conduction and reverse recovery of the parasitic pn diode internal to a MOSFET. Either the drive circuit or the controller used must insure that both FETs are not on simultaneously; this would place a very low resistance path from the input to ground and destructive currents could flow in the FETs. A small amount of deadtime is necessary.

To explain the reverse recovery problem, realize that in normal operation the internal diode of Q2 conducts for a short period at the beginning of the OFF state during the deadtime. MOSFET Q2 is then turned on at the end of the deadtime and its internal diode turns off. But for duty cycles approaching 1 (and very short conduction time for Q2) Q2 may not be turned on after the deadtime. In that case, the internal diode of Q2 is still conducting at the beginning of a new ON state when MOSFET Q1 is turned on. Increased power dissipation due to the diode reverse recovery current can occur if this happens.

Another characteristic of the synchronous buck power stage is that it always operates in continuous conduction mode (CCM) because current can reverse in Q2. Thus the voltage conversion relationship and the duty-cycle-to-output voltage transfer function for the synchronous buck power stage are the same as for the CCM buck power stage.

A simplified schematic of the Synchronous Buck power stage with a drive circuit block included is shown in Figure 7. Both power switches are n-channel MOSFETs. Sometimes, a p-channel FET is used for Q1, but Q2 is almost always an n-channel FET.

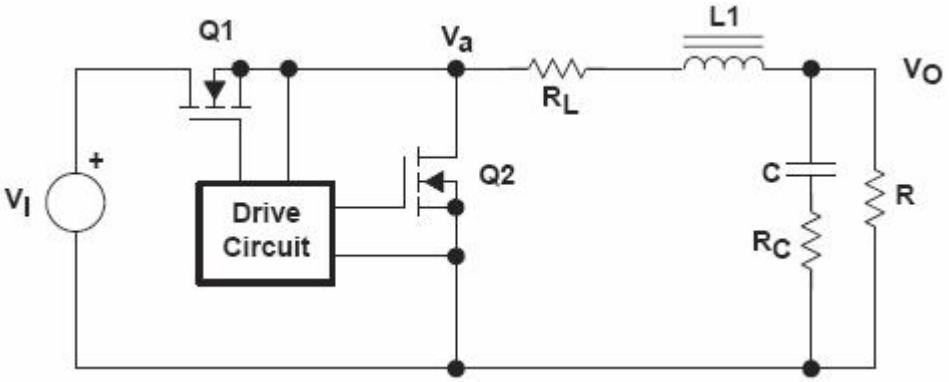

Figure 15. Synchronous Buck Power Stage Schematic

An example design using a synchronous buck power stage and the TL5001 controller is given in SLVP089 Synchronous Buck Converter Evaluation Module User's Guide, Texas Instruments Literature Number SLVU001A

Another example design using a synchronous buck power stage and the TPS5210 controller is given in the Application Report Designing Fast Response Synchronous Buck Regulators Using the TPS5210, TI Literature Number SLVA044.
A third example design using a synchronous buck power stage and the TPS5633 controller is given in Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs User's Guide, Texas Instruments Literature Number SLVU007.

4.2 Forward Converter Power Stage

A transformer-coupled variation of the traditional buck power stage is the forward converter power stage. The power switch is on the primary side of an isolation transformer and a forward rectifier and a catch rectifier are on the secondary side of the isolation transformer. This power stage provides electrical isolation of the input voltage from the output voltage. Besides providing electrical isolation, the isolation transformer can perform step-down (or step-up) of the input voltage to the secondary. The transformer turns ratio can be designed so that reasonable duty cycles are obtained for almost any input voltage/output voltage combination thus avoiding extremely small or extremely high duty cycle values.

The forward converter power stage is very popular in 48-V input telecom applications and 110-VAC or 220-VAC off-line applications for output power levels up to approximately 250

Watts. The exact power rating of the forward converter power stage, of course, is dependent on the input voltage/output voltage combination, its operating environment and many other factors. The capability of obtaining multiple output voltages from a single power stage is another advantage of the forward converter power stage.

A simplified schematic of the forward converter power stage is shown in Figure 16. Not shown in the schematic but necessary for operation is a means of resetting the transformer, T1. There are many ways to accomplish this but a complete discussion is beyond the scope of this report.

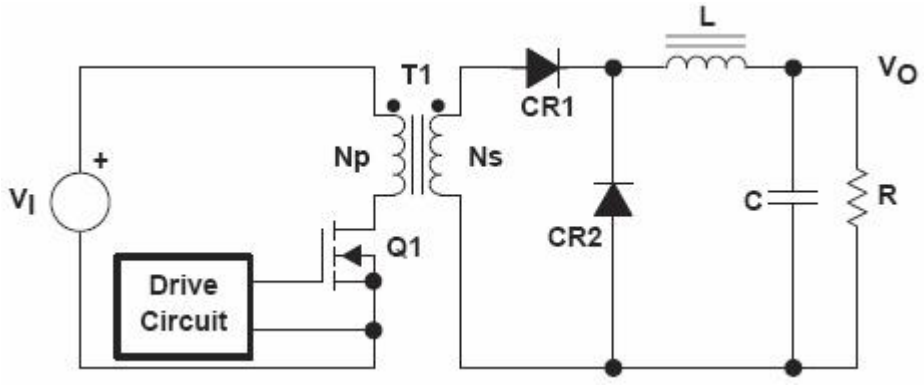

Figure 16. Forward Converter Power Stage Schematic

The simplified voltage conversion relationship for the forward converter power stage operating in CCM is given by:

$$V_O = V_I \times \frac{N_s}{N_p} \times D$$

The simplified voltage conversion relationship for the forward converter power stage operating in DCM is given by:

$$V_O = V_I \times \frac{N_s}{N_p} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_s}$$

The simplified duty-cycle-to-output transfer function for the forward converter power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = V_I \times \frac{N_s}{N_p} \times \frac{R}{R + R_L} \times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

Other power stages which are also variations of the buck power stage include but are not limited to the half-bridge, the full-bridge, and the push-pull power stages.

3.2.1.5 5 Component Selection

This section presents a discussion of the function of each of the main components of the buck power stage. The electrical requirements and applied stresses are given for each power stage component.
The completed power supply, made up of a power stage and a control circuit, usually must meet a set of minimum performance requirements. This set of requirements is usually referred to as the power supply specification. Many times, the power supply specification determines individual component requirements.

3.2.1.5.1 5.1 Output Capacitance

In switching power supply power stages, the function of output capacitance is to store energy. The energy is stored in the capacitor's electric field due to the voltage applied. Thus, qualitatively, the function of a capacitor is to attempt to maintain a constant voltage. The value of output capacitance of a Buck power stage is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually already determined, the series impedance of the capacitor primarily determines the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The following gives guidelines for output capacitor selection.

For continuous inductor current mode operation, to determine the amount of capacitance needed as a function of inductor current ripple, DIL , switching frequency, fS, and desired output voltage ripple, DVO, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance.

$$C \geq \frac{\Delta I_L}{8 \times f_S \times \Delta V_O}$$

where DIL is the inductor ripple current defined in section 2.1.

$$C \geq \frac{I_{O(Max)} \times \left(1 - \frac{I_{O(Max)}}{\Delta I_L}\right)^2}{f_S \times \Delta V_O}$$

For discontinuous inductor current mode operation, to determine the amount of capacitance needed as a function of inductor current ripple, DIL , output current IO, switching frequency, fS, and output voltage ripple, DVO, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance.

where DIL is the inductor ripple current defined in section 2.2.

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected.
For both continuous or discontinuous inductor current mode operation and assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the ripple to DVO V peak-to-peak is:

$$ESR \leq \frac{\Delta V_O}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Referring to Figure 3, the output capacitor ripple current is the inductor current, IL, minus the output current, IO.
The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{C\,RMS} = \Delta I_L \frac{\sqrt{3}}{6} = \Delta I_L (0.289).$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

For some high-performance applications such as a synchronous buck hysteretic regulator controlled by the TPS5210 from Texas Instruments, the output capacitance is selected to provide satisfactory load transient response, because the peak-to-peak output voltage ripple is determined by the TPS5210 controller.
For more information, see the Application Report Designing Fast Response Synchronous Buck Regulators Using the TPS5210, TI Literature Number SLVA044.
Three capacitor technologies—low-impedance aluminum, organic semiconductor, and solid tantalum—are suitable for low-cost commercial applications. Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but ESR is higher than the other two.
Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds—a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

3.2.1.5.2 5.2 Output Inductance

In switching power supply power stages, the function of inductors is to store energy. The energy is stored in their magnetic field due to the current flowing. Thus, qualitatively, the function of an inductor is usually to attempt to maintain a constant current or sometimes to limit the rate of change of current flow.

The value of output inductance of a buck power stage is generally selected to limit the peak-to-peak ripple current flowing in it. In doing so, the power stage's mode of operation, continuous or discontinuous, is determined. The inductor ripple current is directly proportional to the applied voltage and the time that the voltage is applied, and it is inversely proportional to its inductance. This was explained in detail previously.
Many designers prefer to design the inductor themselves but that topic is beyond the scope of this report. However, the following discusses the considerations necessary for selecting the appropriate inductor.

In addition to the inductance, other important factors to be considered when selecting the inductor are its maximum dc or peak current and maximum operating frequency. Using the inductor within its dc current rating is important to insure that it does not overheat or

saturate. Operating the inductor at less than its maximum frequency rating insures that the maximum core loss is not exceeded, resulting in overheating or saturation.
Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficiently high. Current flowing through an inductor causes power dissipation due to the inductor's dc resistance; the power dissipation is easily calculated. Power is also dissipated in the inductor's core due to the flux swing caused by the ac voltage applied across it but this information is rarely directly given in manufacturer's data sheets. Occasionally, the inductor's maximum operating frequency and/or applied volt-seconds ratings give the designer some guidance regarding core loss. The power dissipation causes a temperature increase in the inductor. Excessive temperature can cause degradation in the insulation of the winding and also cause increased core loss. Care should be exercised to insure all the inductor's maximum ratings are not exceeded.

The loss in the inductor is given by:

$$P_{inductor} = I_{Lrms}^2 \times R_{Cu} + P_{Core} \approx I_O^2 \times R_{Cu} + P_{Core}$$

where, RCu is the winding resistance.

3.2.1.5.3 5.3 Power Switch

In switching power supply power stages, the function of the power switch is to control the flow of energy from the input power source to the output voltage. In a buck power stage, the power switch (Q1 in Figure 1) connects the input to the output filter when the switch is turned on and disconnects when the switch is off. The power switch must conduct the current in the output inductor while on and block the full input voltage when off. Also, the power switch must change from one state to the other quickly in order to avoid excessive power dissipation during the switching transition.
The type of power switch considered in this report is a power MOSFET. Other power devices are available but in most instances, the MOSFET is the best choice in terms of cost and performance (when the drive circuits are considered).
The two types of MOSFET available for use are the n-channel and the p-channel. P-channel MOSFETs are popular for use in buck power stages because driving the gate is simpler than the gate drive required for an n-channel MOSFET.
The power dissipated by the power switch is given by:

$$P_{D(MOSFET)} = I_O^2 \times R_{DS(on)} \times D + \frac{1}{2} \times V_I \times I_O \times \left(t_r + t_f\right) \times f_s + Q_{Gate} \times V_{GS} \times f_s$$

Where:
tr and tf are the MOSFET turn-on and turn-off switching times QGate is the MOSFET gate-to-source capacitance

Other than selecting p-channel or n-channel, other parameters to consider while selecting the appropriate MOSFET are the maximum drain-to-source breakdown voltage, V(BR)DSS, and the maximum drain current, ID(Max). The MOSFET selected should have a V(BR)DSS rating greater than the maximum input voltage, and some margin should be added for transients and spikes. The MOSFET selected should also have an ID(Max) rating of at least two times the maximum power stage output current. However, many times this is not sufficient margin and the MOSFET junction temperature should be calculated to make sure that it is not exceeded. The junction temperature can be estimated as follows:

$$T_J = \cdot T_A + P_D \times R_{\Theta JA}$$

Where:
TA is the ambient or heatsink temperature RΘJA is the thermal resistance from the MOSFET chip to the ambient air or heatsink.

3.2.1.5.4 5.4 Catch Rectifier

The catch rectifier conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low–forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low–voltage outputs is usually a Schottky rectifier. The breakdown voltage must be greater than the maximum input voltage, and some margin should be added for transients and spikes. The current rating should be at least two times the maximum power stage output current (normally the current rating will be much higher than the output current because power and junction temperature limitations dominate the device selection).
The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current for the time that the diode is conducting. The switching losses which occur at the transitions from conducting to nonconducting states are very small compared to conduction losses and are usually ignored.
The power dissipated by the catch rectifier is given by:

$$P_{D(Diode)} = V_D \times I_O \times (1 - D)$$

where VD is the forward voltage drop of the catch rectifier. The junction temperature can be estimated as follows:

$$T_J = \cdot T_A + P_D \times R_{\Theta JA}$$

3.2.1.6 6 Example Designs

An example design using a buck power stage, the TPS2817 MOSFET driver, and the TL5001 controller is given in SLVP097 Buck Converter Evaluation Module User's Guide, Texas Instruments Literature Number SLVU002A. Another example design using a buck power stage and the TL5001 controller is given in SLVP087 Buck Converter Evaluation Module User's Guide, Texas Instruments Literature Number SLVU003A.
A third example design using a buck power stage, the TPS2817 MOSFET driver, and the TL5001 controller is given in SLVP101, SLVP102, and SLVP103 Buck Converter Design Using the TL5001 User's Guide, Texas Instruments Literature Number SLVU005.

3.2.1.7 7 Summary

This application report described and analyzed the operation of the buck power stage. The two modes of operation, continuous conduction mode and discontinuous conduction mode, were examined. Steady-state and small-signal were the two analyses performed on the buck power stage. The synchronous buck power stage and the forward converter power stage were presented as variations of the basic buck power stage and a few of the other possible variations were listed.
The main results of the steady-state analyses are summarized below. The voltage conversion relationship for CCM is:

$$V_O = (V_I - V_{DS}) \times D - V_d \times (1 - D) - I_L \times R_L$$

which simplifies to:

$$V_O = V_I \times D$$

The voltage conversion relationship for DCM is:

$$V_O = V_I \times \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2} \times \frac{R}{R + R_L}}}$$

where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

The DCM voltage conversion relationship can be simplified to:

$$V_O = V_I \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

The major results of the small-signal analyses are summarized below. The small-signal duty-cycle-to-output transfer function for the buck power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = V_I \times \frac{R}{R + R_L} \times \frac{1 + R_C \times C}{1 + s \times \left[C \times \left(R_C + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

The small-signal duty-cycle-to-output transfer function for the buck power stage operating in DCM is given by:

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where

$$G_{do} = \frac{2 \times V_O}{D} \times \frac{1 - M}{2 - M}$$

and

$$\omega_p = \frac{2 - M}{1 - M} \times \frac{1}{R \times C}$$

Also presented were requirements for the buck power stage components based on voltage and current stresses applied during the operation of the buck power stage.
For further study, several references are given in addition to example designs.

3.2.1.8 8 References

AUTOR	TITULO	EDITORIAL
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3.V. Vorperian, R. Tymerski, and F. C. Lee	Equivalent Circuit Models for Resonant and PWM Switches	IEEE Transactions on Power Electronics, Vol. 4, No. 2, pp. 205–214, April 1989.
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3.2.2 Understanding Buck-Boost Power Stages in Switch Mode Power Supplies

By:Everett Rogers System Power

ABSTRACT

A switching power supply consists of the power stage and the control circuit. The power stage performs the basic power conversion from the input voltage to the output voltage and includes switches and the output filter. This report addresses the buck-boost power stage only and does not cover control circuits. Detailed steady-state and small-signal analysis of the buck-boost power stage operating in continuous and discontinuous mode is presented.
Variations in the standard buck-boost power stage and a discussion of power stage component requirements are included.

Contents

3.2.2.1 Introduction

The three basic switching power supply topologies in common use are the buck, boost, and buck-boost. These topologies are nonisolated, i.e., the input and output voltages share a common ground. There are, however, isolated derivations of these nonisolated topologies.
The power supply topology refers to how the switches, output inductor, and output capacitor are connected. Each topology has unique properties. These properties include the steady-state voltage conversion ratios, the nature of the input and output currents, and the character of the output voltage ripple. Another important property is the frequency response of the duty-cycle-to-output-voltage transfer function.

The buck-boost is a popular nonisolated, inverting power stage topology, sometimes called a step-up/down power stage. Power supply designers choose the buck-boost power stage because the output voltage is inverted from the input voltage, and the output voltage can be either higher or lower than the input voltage. The topology gets its name from producing an output voltage that can be higher (like a boost power stage) or lower (like a buck power stage) in magnitude than the input voltage. However, the output voltage is opposite in polarity from the input voltage. The input current for a buck-boost power stage is discontinuous or pulsating due to the power switch (Q1) current that pulses from zero to IL every switching cycle. The output current for a buck-boost power stage is also discontinuous or pulsating. This is because the output diode only conducts during a portion of the switching cycle. The output capacitor supplies the entire load current for the rest of the switching cycle. This report describes steady state operation of the buck-boost converter in continuous-mode and discontinuous-mode operation with ideal waveforms given. The duty-cycle-to-outputvoltage transfer function is given after an introduction of the PWM switch model. Figure 1 shows a simplified schematic of the buck-boost power stage with a drive circuit block included. The power switch, Q1, is an n-channel MOSFET. The output diode is CR1. The inductor, L, and capacitor, C, make up the effective output filter. The capacitor ESR, *RC*, (equivalent series resistance) and the inductor DC resistance, *RL*, are included in the analysis. The resistor, *R*, represents the load seen by the power stage output.

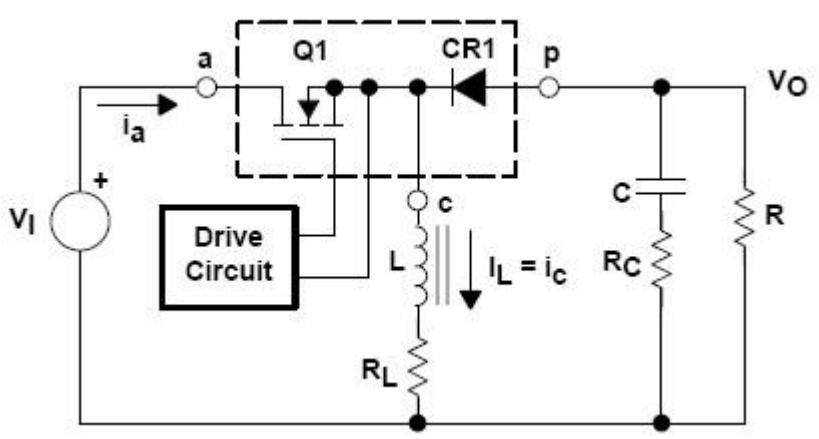

Figure 1. Buck-Boost Power Stage Schematic

During normal operation of the buck-boost power stage, Q1 is repeatedly switched on and off with the on- and off-times governed by the control circuit. This switching action gives rise to a train of pulses at the junction of Q1, CR1, and L. Although the inductor, L, is connected to the output capacitor, C, only when CR1 conducts, an effective L/C output filter is formed. It filters the train of pulses to produce a DC output voltage.

3.2.2.2 Buck-Boost Stage Steady-State Analysis

A power stage can operate in continuous or discontinuous inductor current mode. Continuous inductor current mode is characterized by current flowing continuously in the inductor during the entire switching cycle in steady-state operation. Discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. The two different modes are discussed in greater detail later and design guidelines for the inductor value to maintain a chosen mode of operation as a function of rated load are given. It is very desirable for a converter to stay in one mode only over its expected operating conditions because the power stage frequency response changes significantly between the two different modes of operation.

For this analysis, an n-channel power MOSFET is used and a positive voltage, *VGS(ON)*, is applied from the Gate to the Source terminals of Q1 by the drive circuit to turn ON the FET.

The advantage of using an n-channel FET is its lower *RDS(on)* but the drive circuit is more complicated because a floating drive is required. For the same die size, a p-channel FET has a higher *RDS(on)* but usually does not require a floating drive circuit.

The transistor Q1 and diode CR1 are drawn inside a dashed-line box with terminals labelled a, p, and c. This is explained fully in the *Buck-Boost Power Stage Modeling* section.

2.1 Buck-Boost Steady-State Continuous Conduction Mode Analysis

The following is a description of steady-state operation in continuous conduction mode. The main goal of this section is to provide a derivation of the voltage conversion relationship for the continuous conduction mode buck-boost power stage. This is important because it shows how the output voltage depends on duty cycle and input voltage or conversely, how the duty cycle can be calculated based on input voltage and output voltage. Steady-state implies that the input voltage, output voltage, output load current, and duty-cycle are fixed and not varying. Capital letters are generally given to variable names to indicate a steady-state quantity.

In continuous conduction mode, the buck-boost converter assumes two states per switching cycle. The ON State is when Q1 is ON and CR1 is OFF. The OFF State is when Q1 is OFF and CR1 is ON. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuit during each state. The circuit diagram for each of the two states is shown in Figure 2.

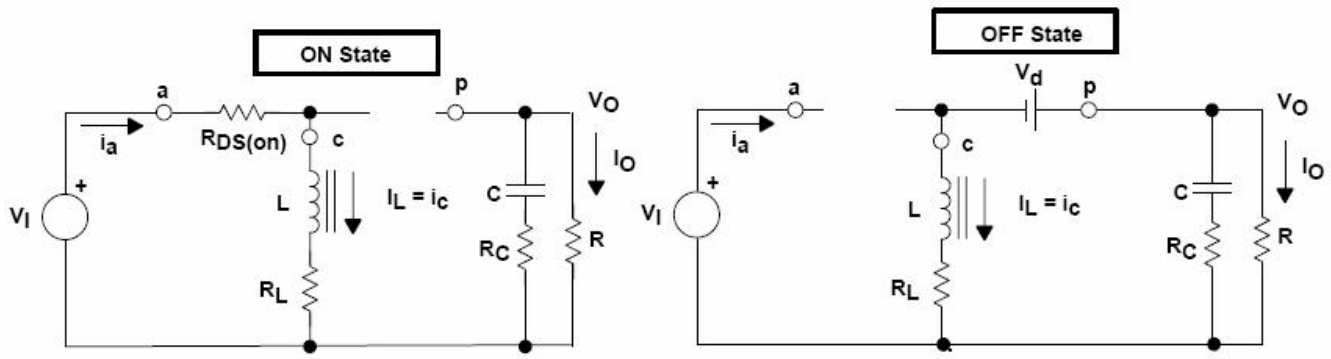

Figure 2. Buck-Boost Power Stage States

The duration of the ON state is *D* × *TS* = *TON* where *D* is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, *Ts*. The duration of the OFF state is called *TOFF*. Since there are only two states per switching cycle for continuous conduction mode, *TOFF* is equal to *(1–D)* × *TS*. The quantity *(1–D)* is sometimes called *D′*. These times are shown along with the waveforms in Figure 3.

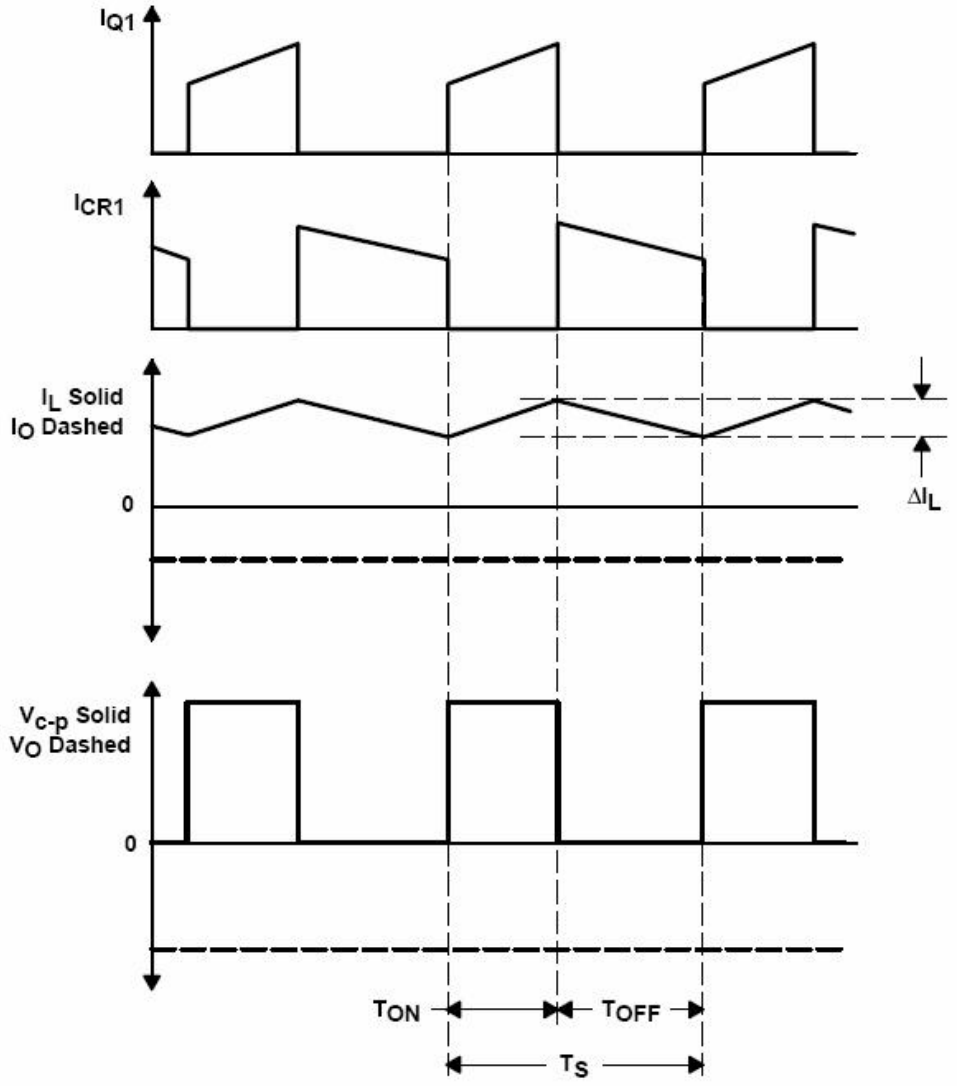

Figure 3. Continuous Mode Buck-Boost Power Stage Waveforms

Referring to Figure 2, during the ON state, Q1 presents a low resistance, *RDS(on)*, from its drain to source and exhibits a small voltage drop of *VDS=IL* × *RDS(on)*. There is also a small voltage drop across the dc resistance of the inductor equal to *IL* × *RL*. Thus, the input voltage, *VI*, minus losses, (*VDS* + *IL* × *RL*), is applied across the inductor, L. CR1 is OFF during this time because it is reverse biased. The inductor current, *IL*, flows from the input source, *VI* , through Q1 and to ground. During the ON state, the voltage applied across the inductor is constant and equal to *VI* – *VDS* – *IL* × *RL*. Adopting the polarity convention for the current *IL* shown in Figure 2, the inductor current increases as a result of the applied voltage.

Also, since the applied voltage is essentially constant, the inductor current increases linearly. This increase in inductor current during *TON* is illustrated in Figure 3.

The amount that the inductor current increases can be calculated by using a version of the familiar relationship:

$$v_L = L \times \frac{di_L}{dt} \Rightarrow \Delta I_L = \frac{v_L}{L} \times \Delta T$$

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{V_I - \left(V_{DS} + I_L \times R_L\right)}{L} \times T_{ON}$$

This quantity, Δ*IL(+)*, is referred to as the inductor ripple current. Also notice that during this period, all of the output load current is supplied by the output capacitor, C.

Referring to Figure 2, when Q1 is OFF, it presents a high impedance from its drain to source. Therefore, since the current flowing in the inductor L cannot change instantaneously, the current shifts from Q1 to CR1. Due to the decreasing inductor current, the voltage across the inductor reverses polarity until rectifier CR1 becomes forward biased and turns ON. The voltage applied across L becomes (*VO* – *Vd* – *IL* × *RL)* where the quantity, *Vd*, is the forward voltage drop of CR1. The inductor current, *IL*, now flows from the output capacitor and load resistor combination through CR1 and to ground. Notice that the orientation of CR1 and the direction of current flow in the inductor means that the current flowing in the output capacitor and load resistor combination causes *VO* to be a negative voltage. During the OFF state, the voltage applied across the inductor is constant and equal to *(VO – Vd – IL × RL)*. Maintaining our same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the ON time), because the output voltage VO is negative. Hence, the inductor current decreases during the OFF time. Also, since the applied voltage is essentially constant, the inductor current decreases linearly. This decrease in inductor current during *TOFF* is illustrated in Figure 3.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{-\left(V_O - V_d - I_L \times R_L\right)}{L} \times T_{OFF}$$

This quantity, $\Delta I_L(-)$, is also referred to as the inductor ripple current.
In steady state conditions, the current increase, $\Delta I_L(+)$, during the ON time and the current decrease during the OFF time, $\Delta I_L(-)$, must be equal. Otherwise, the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. Therefore, these two equations can be equated and solved for *Vo* to obtain the continuous conduction mode buck-boost voltage conversion relationship:
Solving for *Vo*:

$$V_O = -\left[\left(V_I - V_{DS}\right) \times \frac{T_{ON}}{T_{OFF}} - V_d - I_L \times R_L \times \frac{T_{ON} + T_{OFF}}{T_{OFF}}\right]$$

And, substituting *TS* for *TON + TOFF*, and using *D = TON/TS* and *(1–D) = TOFF/TS*, the steady-state equation for *VO* is:

$$V_O = -\left[\left(V_I - V_{DS}\right) \times \frac{D}{1-D} - V_d - \frac{I_L \times R_L}{1-D}\right]$$

Notice that in simplifying the above, *TON + TOFF* is assumed to be equal to *TS*. This is true only for continuous conduction mode as we will see in the discontinuous conduction mode analysis.

An important observation should be made here: Setting the two values of ΔIL equal to each other is precisely equivalent to *balancing the volt-seconds* on the inductor. The volt-seconds applied to the inductor is the product of the voltage applied and the time that the voltage is applied. This is the best way to calculate unknown values such as V*O* or *D* in terms of known circuit parameters, and this method will be applied repeatedly in this paper. Volt-second balance on the inductor is a physical necessity and should be comprehended at least as well as Ohms Law.
In the above equations for $\Delta IL(+)$ and $\Delta IL(-)$, the output voltage was implicitly assumed to be constant with no AC ripple voltage during the ON time and the OFF time. This is a common simplification and involves two separate effects. First, the output capacitor is assumed to be large enough that its voltage change is negligible. Second, the voltage due to the capacitor ESR is also assumed to be negligible. These assumptions are valid because the AC ripple voltage is designed to be much less than the DC part of the output voltage.
The above voltage conversion relationship for *VO* illustrates the fact that *VO* can be adjusted by adjusting the duty cycle, *D*. This relationship approaches zero as *D* approaches zero and increases without bound as *D* approaches 1. A common simplification is to assume *VDS*, *Vd*, and *RL* are small enough to ignore. Setting *VDS*, *Vd*, and *RL* to zero, the above equation simplifies considerably to:

Ecuacion 6

$$V_O = -V_I \times \frac{D}{1-D}$$

A simplified, qualitative way to visualize the circuit operation is to consider the inductor as an energy storage element. When Q1 is on, energy is added to the inductor. When Q1 is off, the inductor delivers some of its energy to the output capacitor and load. The output voltage is controlled by setting the on-time of Q1. For example, by increasing the on-time of Q1, the amount of energy delivered to the inductor is increased. More energy is then delivered to the output during the off-time of Q1 resulting in an increase in the output voltage.
Unlike the buck power stage, the average of the inductor current is not equal to the output current. To relate the inductor current to the output current, referring to Figures 2 and 3, note that the inductor delivers current to the output only during the off state of the power stage.
This current averaged over a complete switching cycle is equal to the output current because the average current in the output capacitor must be equal to zero.

The relationship between the average inductor current and the output current for the continuous mode buck-boost power stage is given by:

$$I_{L(Avg)} \times \frac{T_{OFF}}{T_S} = I_{L(Avg)} \times (1-D) = -I_O$$

or

$$I_{L(Avg)} = \frac{-I_O}{(1-D)}$$

Another important observation is that the average inductor current is proportional to the output current, and since the inductor ripple current, ΔIL, is independent of output load current, the minimum and the maximum values of the inductor current track the average inductor current exactly. For example, if the average inductor current decreases by 2 A due to a load current decrease, then the minimum and maximum values of the inductor current decrease by 2 A (assuming continuous conduction mode is maintained).
The forgoing analysis was for the buck-boost power stage operation in continuous inductor current mode. The next section is a description of steady-state operation in discontinuous conduction mode. The main result is a derivation of the voltage conversion relationship for the discontinuous conduction mode buck-boost power stage.

2.2 Buck-Boost Steady-State Discontinuous Conduction Mode Analysis

We now investigate what happens when the load current is decreased and the conduction mode changes from continuous to discontinuous. Recall for continuous conduction mode, the average inductor current tracks the output current, i.e. if the output current decreases, then so does the average inductor current. In addition, the minimum and maximum peaks of the inductor current follow the average inductor current exactly.

If the output load current is reduced below the critical current level, the inductor current will be zero for a portion of the switching cycle. This should be evident from the waveforms shown in Figure 3, since the peak to peak amplitude of the ripple current does not change with output load current. In a buck-boost power stage, if the inductor current attempts to fall below zero, it just stops at zero (due to the unidirectional current flow in CR1) and remains there until the beginning of the next switching cycle. This operating mode is called discontinuous conduction mode. A power stage operating in discontinuous conduction mode has three unique states during each switching cycle as opposed to two states for continuous conduction mode. The inductor current condition where the power stage is at the boundary between continuous and discontinuous mode is shown in Figure 4. This is where the inductor current just falls to zero and the next switching cycle begins immediately after the current reaches zero. Note that the absolute values of IO and IO(Crit) are shown in Figure 4 because IO and IL have opposite polarities.

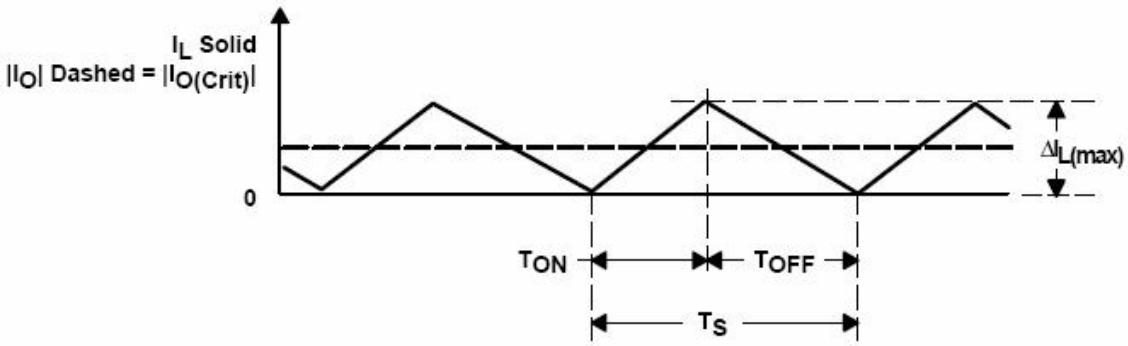

Figure 4. Boundary Between Continuous and Discontinuous Mode

Further reduction in output load current puts the power stage into discontinuous conduction mode. This condition is illustrated in Figure 5. The discontinuous mode power stage frequency response is quite different from the continuous mode frequency response and is given in the Buck-Boost Power Stage Modeling section. Also, the input to output relationship is quite different as shown in the following derivation.

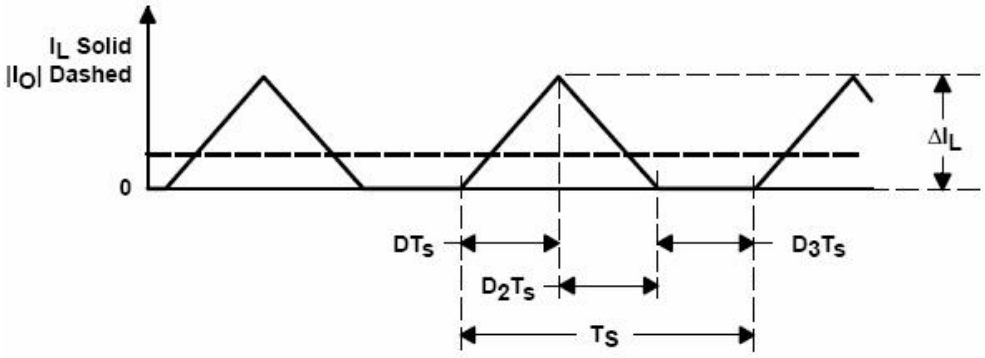

Figure 5. Discontinuous Current Mode

To begin the derivation of the discontinuous conduction mode buck-boost power stage voltage conversion ratio, recall that there are three unique states that the converter assumes during discontinuous conduction mode operation. The ON State is when Q1 is ON and CR1 is OFF. The OFF State is when Q1 is OFF and CR1 is ON. The IDLE state is when both Q1 and CR1 are OFF. The first two states are identical to those of the continuous mode case and the circuits of Figure 2 are applicable except that *TOFF* ≠ *(1–D)* × *TS*. The remainder of the switching cycle is the IDLE state. In addition, the DC resistance of the output inductor, the output diode forward voltage drop, and the power MOSFET ON-state voltage drop are all assumed to be small enough to omit.

The duration of the ON state is *TON = D* × *TS* where *D* is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, *Ts*. The duration of the OFF state is *TOFF = D2* × *TS*. The IDLE time is the remainder of the switching cycle and is given as *TS – TON – TOFF = D3* × *TS*. These times are shown with the waveforms in Figure 6.

Without going through the detailed explanation as before, the equations for the inductor current increase and decrease are given below.

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{V_I}{L} \times T_{ON} = \frac{V_I}{L} \times D \times T_S = I_{PK}$$

The ripple current magnitude, Δ*IL(+)*, is also the peak inductor current, *Ipk* because in discontinuous mode, the current starts at zero each cycle.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{-V_O}{L} \times T_{OFF} = \frac{-V_O}{L} \times D_2 \times T_S$$

As in the continuous conduction mode case, the current increase, Δ*IL(+)*, during the ON time and the current decrease during the OFF time, Δ*IL(–)*, are equal. Therefore, these two equations can be equated and solved for *VO* to obtain the first of two equations to be used to solve for the voltage conversion ratio:

$$V_O = -V_I \times \frac{T_{ON}}{T_{OFF}} = -V_I \times \frac{D}{D_2}$$

Now we calculate the output current (the output voltage *VO* divided by the output load *R*). It is the average over one switching cycle of the inductor current during the time when CR1 conducts (D2 × TS).

$$\frac{V_O}{R} = I_O = \frac{1}{T_S} \times \left[\frac{-I_{PK}}{2} \times D_2 \times T_S \right]$$

Now, substitute the relationship for *IPK* (ΔIL(+)) into the above equation to obtain:

$$\frac{V_O}{R} = I_O = \frac{1}{T_S} \times \left[\frac{1}{2} \times (-1) \times \left(\frac{V_I}{L} \times D \times T_S \right) \times D_2 \times T_S \right]$$

$$\frac{V_O}{R} = \frac{-V_I \times D \times D_2 \times T_S}{2 \times L}$$

We now have two equations, the one for the output current (V_O divided by R) just derived and the one for the output voltage, both in terms of V_I, D, and D_2. We now solve each equation for D_2 and set the two equations equal to each other. Using the resulting equation, an expression for the output voltage, V_O, can be derived.

The discontinuous conduction mode buck-boost voltage conversion relationship is given by:

Ecuacion 14

$$V_O = -V_I \times \frac{D}{\sqrt{K}}$$

Where K is defined as

$$K = \frac{2 \times L}{R \times T_S}$$

The above relationship shows one of the major differences between the two conduction modes. For discontinuous conduction mode, the voltage conversion relationship is a function of the input voltage, duty cycle, power stage inductance, the switching frequency, and the output load resistance. For continuous conduction mode, the voltage conversion relationship is only dependent on the input voltage and duty cycle.

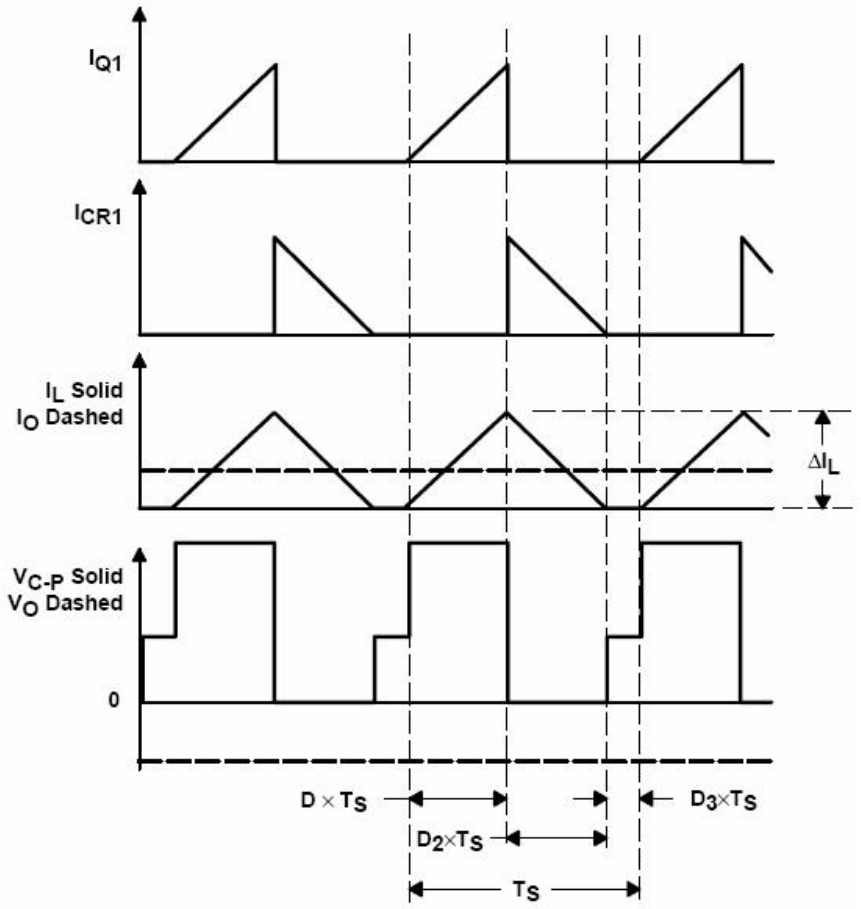

Figure 6. Discontinuous Mode Buck-Boost Converter Waveforms

In typical applications, the buck-boost power stage is operated in either continuous conduction mode or discontinuous conduction mode. For a particular application, one conduction mode is chosen and the power stage is designed to maintain the same mode. The next section gives inductance relationships for the power stage that allow it to operate in only one conduction mode, given ranges for input and output voltage and output load current.

2.3 Critical Inductance

The previous analyses for the buck-boost converter have been for continuous and discontinuous conduction modes of steady-state operation. The conduction mode of a converter is a function of input voltage, output voltage, output current, and the value of the inductor. A buck-boost converter can be designed to operate in continuous mode for load currents above a certain level, usually 5% to 10% of full load. Usually, the input voltage range, the output voltage, and load current are defined by the converter specification. This leaves the inductor value as the design parameter to maintain continuous conduction mode.
The minimum value of inductor to maintain continuous conduction mode can be determined by the following procedure.

First, define *IO(Crit)* as the minimum output current to maintain continuous conduction mode, normally referred to as the critical current. This value is shown in Figure 4. Since we are working toward a minimum value for the inductor, it is more straightforward to perform the derivation using the inductor current. The minimum average inductor current to maintain continuous conduction mode is given by:

$$I_{L(min-avg)} = \frac{\Delta I_L}{2} = I_{O(crit)}$$

Second, calculate L such that the above relationship is satisfied. To solve the above equation, either relationship, $\Delta IL(+)$ or $\Delta IL(-)$ may be used for ΔIL. Note also that either relationship for ΔIL is independent of the output current level. Here, $\Delta IL(+)$ is used. The worst case condition (giving the largest *Lmin*) is at maximum input voltage because this gives the maximum ΔIL.
Now, substituting and solving for *Lmin*:

$$L_{min} \geq \frac{1}{2} \times \left(V_{I(max)} - V_{DS} - I_L \times R_L\right) \times \frac{T_{ON(min)}}{I_{O(crit)}}$$

The above equation can be simplified by ignoring minor parasitic resistances and diode voltage drops, and rearranged for ease of use to:

$$L_{min} \geq \frac{-V_O \times T_S}{2 \times I_{O(crit)}} \times \frac{V_{I(max)}}{\left(V_O - V_{I(max)}\right)}$$

Using the inductor value just calculated will guarantee continuous conduction mode operation for output load currents above the critical current level, *IO(crit)* .

3.2.2.3 3 Buck-Boost Power Stage Small Signal Modeling

We now switch gears, moving from a detailed circuit oriented analysis approach to more of a system level investigation of the buck-boost power stage. This section presents techniques to assist the power supply designer in accurately modeling the power stage as a component of the control loop of a buck-boost power supply. The three major components of the power supply control loop (i.e., the power stage, the pulse width modulator, and the error amplifier) are shown in block diagram form in Figure 7.

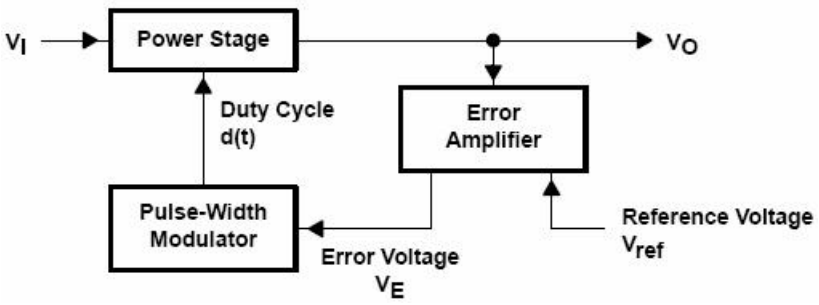

Figure 7. Power Supply Control Loop Components

Modeling the power stage presents one of the main challenges to the power supply designer. A popular technique involves modeling only the switching elements of the power stage. An equivalent circuit for these elements is derived and is called the *PWM Switch Model* where PWM is the abbreviation for the pulse width modulated. This approach is presented here. As shown in Figure 7, the power stage has two inputs: the input voltage and the duty cycle.
The duty cycle is the control input, i.e., this input is a logic signal which controls the switching action of the power stage and hence the output voltage. Most power stages have a nonlinear voltage conversion ratio versus duty cycle. To illustrate this nonlinearity, a graph of the steady-state voltage conversion ratio for a buck-boost power stage operating in continuous conduction mode as a function of steady-state duty cycle, D, is shown in Figure 8.
The nonlinear characteristics are a result of the switching action of the power stage switching components, Q1 and CR1. It was observed in reference [5] that the only nonlinear components in a power stage are the switching devices; the remainder of the circuit consists of linear elements. It was also shown in reference [5] that a linear model of only the nonlinear components could be derived by averaging the voltages and currents associated with these nonlinear components over one switching cycle. The model is then substituted into the original circuit for analysis of the complete power stage. Thus, a model of the switching devices is given and is called the *PWM switch* model.

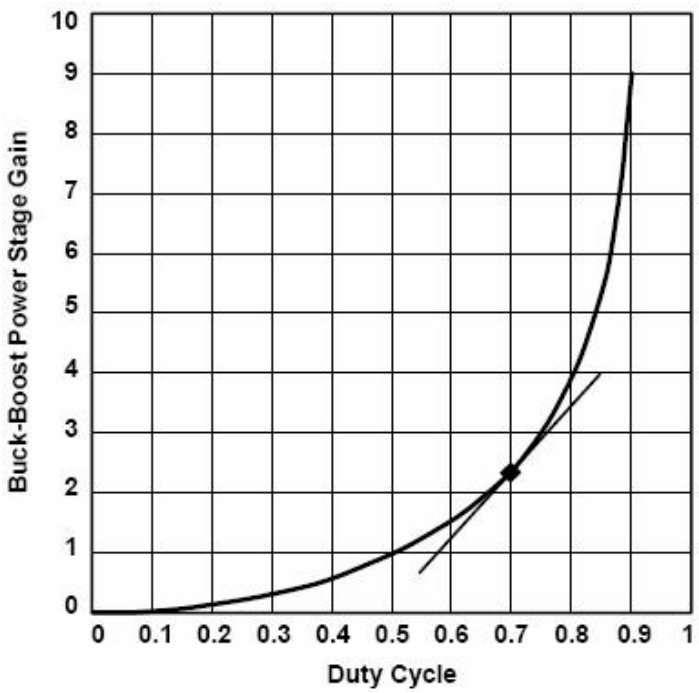

Figure 8. Buck-Boost Power Stage Gain vs Duty Cycle

The basic objective behind modeling power stages is to represent the non-linear behavior of power stages as linear about an operating point. We want linearity so that we can apply the many analysis tools available for linear systems. Referring again to Figure 8, if we choose the operating point of $D = 0.7$, a straight line can be constructed that is tangent to the original curve at the point where $D = 0.7$. This is an illustration of linearization about an operating point, a technique used to derive the PWM switch model. Qualitatively, one can see that if the

variations in duty cycle are kept small, a linear model accurately represents the nonlinear behavior of the power stage being analyzed.
Since a power stage can operate in one of two conduction modes, i.e., continuous conduction mode (CCM) or discontinuous conduction mode (DCM), there is a PWM switch model for the two conduction modes. The DCM PWM switch model is derived here. The CCM PWM switch model is derived in the Application Report *Understanding Buck Power Stages in Switchmode Power Supplies*, TI Literature Number SLVA057.

3.1 Buck-Boost Continuous Conduction Mode Small-Signal Analysis

To model the buck-boost power stage operation in CCM, we use the CCM PWM switch model derived in the Application Report *Understanding Buck Power Stages in Switchmode Power Supplies*, TI Literature Number SLVA057. The PWM switch model is inserted into the power stage circuit by replacing the switching elements. The CCM PWM Switch model is shown in Figure 9. This model is useful for determining the dc operating point of a power stage and for finding ac transfer functions of a power stage.
Referring again to Figure 1, the power transistor, Q1, and the catch diode, CR1, are drawn inside a dashed-line box. These are the components that will be replaced by the PWM switch equivalent circuit. Terminal labels a (active), p (passive), and c (common) are used for the PWM switch model.

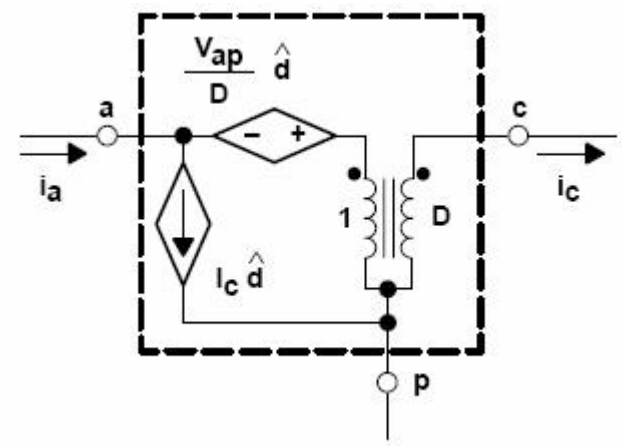

Figure 9. DC and Small Signal CCM PWM Switch Model

The a terminal is the terminal connected to the active switch. The p terminal is the terminal of the passive switch. The c terminal is the terminal that is common to both the active and passive switches. The three commonly used power stage topologies all contain active and passive switches, and the above terminal definitions can be used. In addition, substituting the PWM switch model (that we will derive) into other power stage topologies also produces a valid model for that particular power stage. To use the PWM switch model in other power stages, just substitute the model shown in Figure 9 into the power stage in the appropriate orientation.

In the PWM switch model of Figure 9 and subsequent occurrences of the model, the capital letters indicate steady-state (or dc) quantities dependent on the operating point of the circuit under study. The lowercase letters indicate time varying quantities and can indicate a quantity with a dc component and an ac component. The lowercase letters with a caret (hat) indicate the small ac variations of that particular variable. For example, *D* represents the steady-state duty cycle, *d* ^ represents small ac variations of the duty cycle, and *d* or *d(t)* represents the complete duty cycle including any dc component and ac variations.

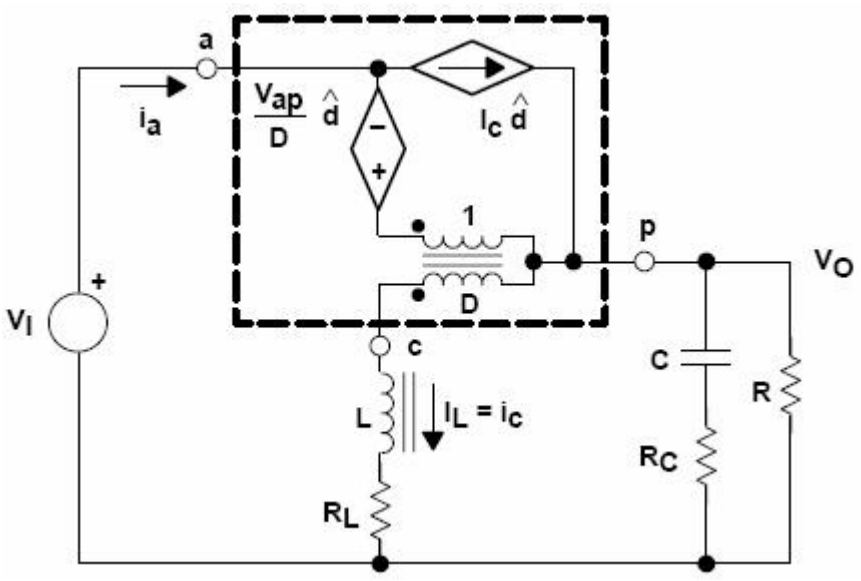

Figure 10. CCM Buck-Boost Small Signal AC Power Stage Model

An example dc analysis is given to illustrate how simple power stage analysis becomes with the PWM switch model. For dc analysis, *d* ^ is zero, L is a short and C is an open. Then by a simple loop equation we get:

Ecuacion 19

$$-V_I + \frac{V_{ac}}{D} + V_O = 0$$

By using the following relationships

$$I_L = \frac{-I_O}{1-D}$$

$$I_O = \frac{V_O}{R}$$

and writing another loop to solve for VCP, we get:

$$V_{cp} = -V_O \times \left(1 + \frac{R_L}{R \times (1-D)}\right)$$

Using the two loop equations, we solve them to get the steady-state voltage conversion relationship for the buck-boost power stage operating in CCM and taking the inductor dc resistance, RL, into account:

$$V_O = -V_I \times \frac{D}{1-D} \times \frac{1}{1+\frac{R_L}{R\times(1-D)^2}}$$

The above equation is usually expressed as a ratio of the output voltage, *VO*, to the input voltage, *VI* , and is usually called *M* as shown below:

$$M = \frac{V_O}{V_I} = -\frac{D}{1-D} \times \frac{1}{1+\frac{R_L}{R\times(1-D)^2}}$$

Which, when RL = 0, as assumed earlier, is equal to the steady-state I/O transfer function previously calculated. With the PWM switch parameters *Vap* and *Ic* determined from the dc analysis, an ac analysis can be performed. For ac analysis, the following transfer functions can be calculated: open-loop line-to-output, open-loop input impedance, open-loop output impedance, and open-loop control-to-output. The control-to-output, or duty-cycle-to-output, is the transfer function most used for control loop analysis. To determine this transfer function, first use the results from the dc analysis for operating point information. This information determines the parameter values of the dependent sources; for example,

$$V_{ap} = V_I - V_O = V_I \times (1-M)$$

and

$$I_c = I_L = \frac{-I_O}{1-D} = \frac{-V_O}{R\times(1-D)} = \frac{-M\times V_I}{R\times(1-D)}$$

The above two equations are then used with loop equations to derive the duty-cycle-to-output voltage transfer function. Then set the input voltage equal to zero because we only want the ac component of the transfer function. Without going through all the details, it can be shown that the transfer function can be put in the following form:

$$\frac{\hat{v}_O}{\hat{d}}(s) = G_{do} \times \frac{\left(1+\frac{s}{\omega_{z1}}\right)\times\left(1-\frac{s}{\omega_{z2}}\right)}{1+\frac{s}{\omega_o\times Q}+\frac{s^2}{\omega_o^2}}$$

Where:

$$G_{do} \approx \frac{V_I}{(1-D)^2}$$

$$s_{z1} = \frac{1}{R_C \times C}$$

$$s_{z2} \approx \frac{(1-D)^2 \times R}{D \times L}$$

$$\omega_o \approx \frac{1-D}{\sqrt{L \times C}}$$

$$Q \approx \frac{(1-D) \times R}{\sqrt{\frac{L}{C}}}$$

3.2 Buck-Boost Discontinuous Conduction Mode Small-Signal Analysis

We now continue our discussion of modeling the power stage when it is operating in discontinuous conduction mode (DCM). This mode is quite different from continuous conduction mode just covered. We begin with the derivation of the PWM switch model for DCM for the buck-boost power stage. This derivation can also be found in [4]. The waveforms that are averaged are the voltage across Q1, *vac*, the voltage across CR1, *vcp*, the current in Q1, *ia* and the current in CR1, *ip*. The waveforms are shown in Figure 6.

We first state some basic relationships that are used repeatedly. The terminal currents averaged over one switching cycle are given by:

$$\langle i_a \rangle = \frac{i_{pk}}{2} \times d$$

$$\langle i_p \rangle = \frac{i_{pk}}{2} \times d_2$$

where variables in brackets (e.g., <ia>) represent quantities that are averaged over one switching cycle.

Since the average over one switching cycle of the voltage across the inductor is zero, the following average voltage relationships hold:

$$\langle v_{ac} \rangle = V_I + (i_c \times R_L)$$

$$\langle v_{cp} \rangle = -V_O - (i_c \times R_L)$$

Ecuacio 28

Since the value of *icRL* is small compared to *VI* and *VO*, ignore these values for modeling the power stage to make the formulae much easier to manipulate. During the time period *d* × *Ts* the current *ia* starts at a value of zero and ends at the value of *ipk*. And since the voltage across the inductor during this time is constant and equal to *VI* = <vac>, the following holds:

$$V_I = L\frac{\Delta i_a}{\Delta t} = L \times \frac{i_{pk}}{d \times T_S} \Rightarrow \langle v_{ac} \rangle = L \times \frac{i_{pk}}{d \times T_S}$$

Similarly, during the time period *d2 Ts*, the current *ip* starts at a value of *ipk* and ends at zero.
Also since the voltage across the inductor is equal to −*VO* = <vcp>, the following holds:

$$V_O = L\frac{\Delta i_p}{\Delta t} = L \times \frac{-i_{pk}}{d2 \times T_S} \Rightarrow \langle v_{cp} \rangle = L \times \frac{i_{pk}}{d2 \times T_S}$$

With the above four equations, we begin with the derivation of the input side (*vac* side) of the PWM switch model.
We solve equation (3) for *ipk* and use *VI* = <vac>, then substitute into equation (1) to get:

$$\langle i_a \rangle = V_I \times \frac{d^2 \times T_S}{2 \times L}$$

We note that the average current flowing into terminal *a* is proportional to the input voltage, *VI*. We define an effective resistance as follows:

Ecuacion 32

$$R_e = \frac{V_I}{\langle i_a \rangle} = \frac{2 \times L}{d^2 \times T_S}$$

Once the input looks like an equivalent resistance, we can also talk about an apparent input power of VI2 /Re which will be used next.
To begin the derivation of the output side (*vcp* side), we start with equation (4), solve equation (3) for *ipk* and substitute back into equation (4), we get:

$$\langle v_{cp} \rangle = \frac{\langle v_{ac} \rangle \times d}{d_2}$$

We next solve the above equation for *d2* and substitute into equation (2) and also use *ipk* [from equation (3)] and substitute into equation (2), we get after rearranging:

$$\langle i_p \rangle = \frac{\langle v_{ac} \rangle^2 \times d^2 \times T_S}{\langle v_{cp} \rangle \times 2 \times L}$$

Finally, we use <vac> = *VI* and substitute in the above equation to get the output side relationship:

$$\langle i_p \rangle \times \langle v_{cp} \rangle = V_I^2 \times \frac{d^2 \times T_S}{2 \times L} = \frac{V_I^2}{R_e}$$

This equation shows that the average output current times the average output voltage is equal to the apparent input power.
Now we can implement the above input and output relationships into an equivalent circuit model. This model is useful for determining the dc operating point of a power supply. The input port is simply modeled with a resistor, Re. The output port is modeled as a dependent power source. This power source delivers power equal to that dissipated by the input resistor, Re. The equivalent circuit can be constructed as shown in Figure 11.

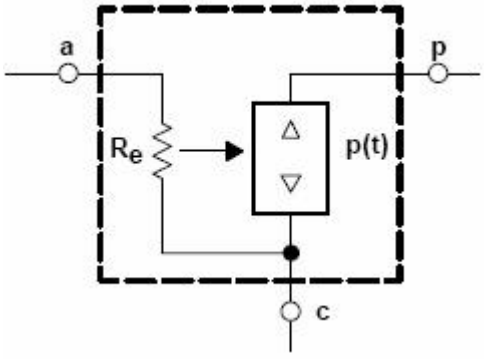

Figure 11. DCM PWM Switch Model

To illustrate discontinuous conduction mode power supply steady-state analysis using this model, we examine the buck-boost converter. The analysis proceeds like the CCM case. The equivalent circuit is substituted into the original circuit. The inductor is treated as a short circuit and the capacitor is treated as an open circuit. The DCM buck-boost converter model schematic is shown in the Figure 12.

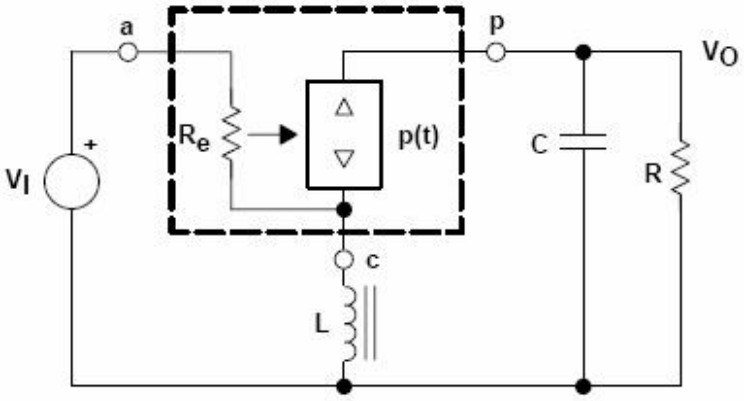

Figure 12. DCM Buck-Boost Converter Model

The apparent power *dissipated* in Re is determined as:

Ecuacion 36

$$P_{Re} = \frac{V_I^2}{R_e}$$

The dependent power source delivers the above amount of power to the output load resistor, R. We can calculate the voltage gain as a function of D by equating the two powers as shown:

$$\frac{V_I^2}{R_e} = \frac{V_O^2}{R}$$

$$\frac{V_O}{V_I} = \pm \sqrt{\frac{R}{R_e}} \text{ (choose the negative root)}$$

$$\sqrt{\frac{R}{R_e}} = \sqrt{\frac{R}{\frac{2 \times L}{D^2 \times T_S}}} = D \sqrt{\frac{R \times T_S}{2 \times L}}$$

The voltage conversion relationship for the DCM buck-boost is given by:

$$\frac{V_O}{V_I} = - D \sqrt{\frac{R \times T_S}{2 \times L}}$$

Recall from earlier that:

$$\frac{V_O}{V_I} = - \frac{D}{\sqrt{K}}$$

and making the substitution in the above equation, the result is identical to that obtained by balancing the inductor volt-seconds in the buck-boost steady-state discontinuous conduction mode analysis section.

The steady state voltage conversion relationship for the DCM buck-boost becomes:

Now, to derive the small signal model, the circuit of Figure 12 is perturbed and linearized following the procedure similar to the one in the CCM derivation. To see the detail of the derivation, the reader is directed to reference [4] for details. The resulting small signal model for the buck-boost power stage operating in DCM is shown in the Figure 13.

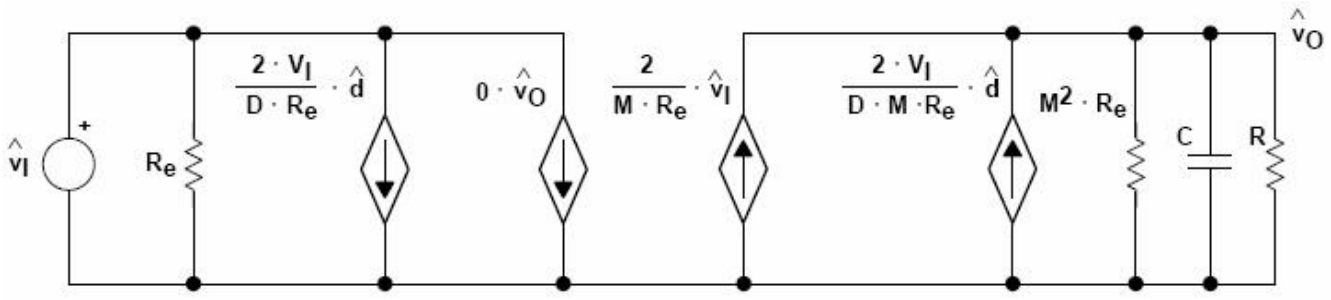

Figure 13. Small Signal DCM Buck-Boost Power Stage Model

The duty-cycle-to-output transfer function for the buck-boost power stage operating in DCM is given by

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where:

$$G_{do} = \frac{V_O}{D}$$

$$D = -M \times \sqrt{K}$$

$$M = \frac{V_O}{V_I}$$

$$K = \frac{2 \times L}{R \times T_S}$$

and

$$\omega_p = \frac{2}{R \times C}$$

The expression for Gdo can be simplified to the following:

$$G_{do} = -V_I \times \sqrt{\frac{R \times T_S}{2 \times L}}$$

3.2.2.4 4 Variations of the Buck-Boost Power Stage

4.1 Flyback Power Stage

A transformer-coupled variation of the traditional buck-boost power stage is the flyback power stage. This power stage operates like the traditional buck-boost power stage except that the single winding inductor is replaced with a two (or more) winding coupled inductor. The power switch, Q1 in Figure 14, applies the input voltage to the primary side (LPRI) of the coupled inductor. Energy is stored until Q1 is turned off. Energy is then delivered to the output capacitor and load resistor combination from the secondary side (LSEC) of the coupled inductor through the output diode CR1. This power stage provides electrical isolation of the input voltage from the output voltage. Besides providing electrical isolation, the isolation transformer can step-down (or step-up) the input voltage to the secondary. The transformer turns ratio can be designed so that reasonable duty cycles are obtained for almost any input voltage/output voltage combination, thus avoiding extremely small or extremely high duty cycle values.
The flyback power stage also eliminates two characteristics which sometimes make the standard buck-boost power stage unattractive; i.e., the output voltage is opposite in polarity from the input voltage and the power switch requires a floating drive. Besides providing isolation, the coupled inductor secondary can be connected to produce an output voltage of either positive or negative polarity. In addition, since the power switch is in series with the primary of the coupled inductor, the power switch can be connected so that the source is ground referenced instead of connecting the drain to the input voltage as in the standard buck-boost power stage.

The flyback power stage is very popular in 48-V input telecom applications and 110-V ac or 220-V ac off-line applications for output power levels up to approximately 50 watts. The exact power rating of the flyback power stage, of course, is dependent on the input voltage/output voltage combination, its operating environment and many other factors. Additional output voltages can be generated easily by simply adding another winding to the coupled inductor along with an output diode and output capacitor. Obtaining multiple output voltages from a single power stage is another advantage of the flyback power stage.
A simplified schematic of the flyback power stage with a drive circuit block included is shown in Figure 14. In the schematic shown, the secondary winding of the coupled inductor is connected to produce a positive output voltage. The power switch, Q1, is an n-channel MOSFET. The diode, CR1, is usually called the output diode. The secondary inductance, LSEC, and capacitor, C, make up the output filter. The capacitor ESR, RC, (equivalent series resistance) is not included. The resistor, R, represents the load seen by the power supply output.

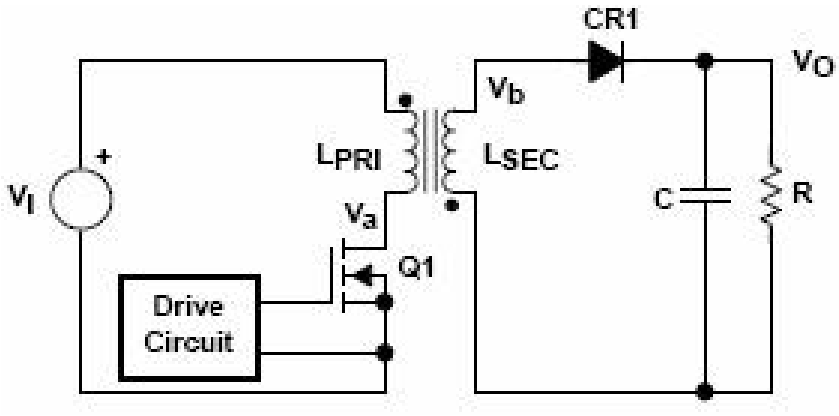

Figure 14. Flyback Power Stage Schematic

The important waveforms for the flyback power stage operating in DCM are shown in Figure 15.

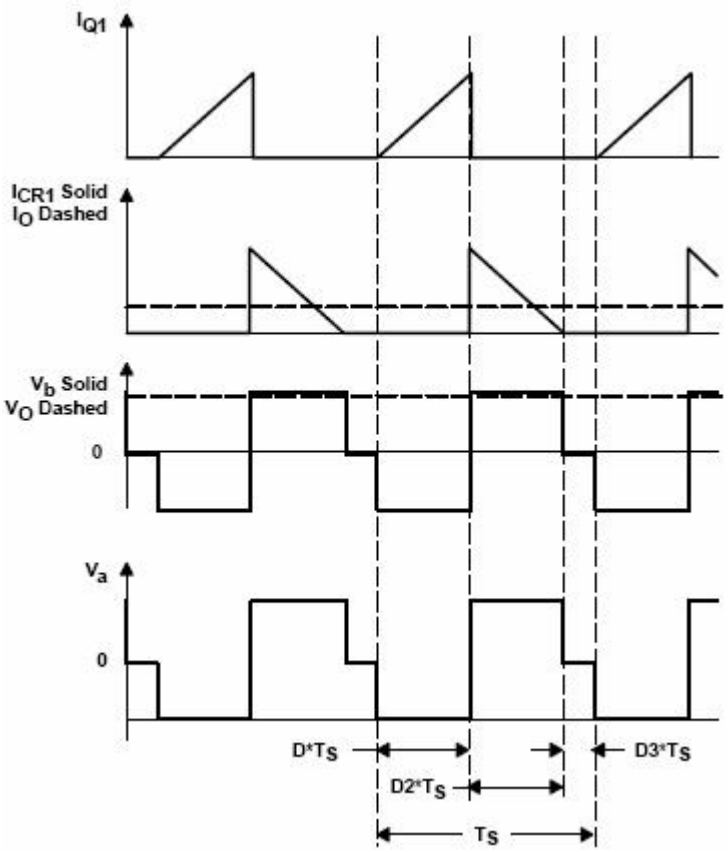

Figure 15. Discontinuous Mode Flyback Waveforms

The simplified voltage conversion relationship for the flyback power stage operating in CCM (ignoring parasitics) is given by:

ecuacion 44

$$V_O = V_I \times \frac{N_S}{N_P} \times \frac{D}{1 - D}$$

The simplified voltage conversion relationship for the flyback power stage operating in DCM (ignoring parasitics) is given by:

$$V_O = V_I \times \frac{N_S}{N_P} \times \frac{D}{\sqrt{K}}$$

Where K is defined as:

$$K = \frac{2 \times L_{SEC}}{R \times T_S}$$

The simplified duty-cycle-to-output transfer function for the flyback power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = G_{do} \times \frac{N_S}{N_P} \times \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \times \left(1 - \frac{s}{\omega_{z2}}\right)}{1 + \frac{s}{\omega_o \times Q} + \frac{s^2}{\omega_o^2}}$$

Where:

$$G_{do} \approx \frac{V_I}{(1 - D)^2}$$

$$\omega_{z1} = \frac{1}{R_C \times C}$$

$$\omega_{z2} \approx \frac{(1 - D)^2 \times R}{D \times L_{SEC}}$$

$$\omega_o \approx \frac{1 - D}{\sqrt{L_{SEC} \times C}}$$

$$Q \approx \frac{(1 - D) \times R}{\sqrt{\frac{L_{SEC}}{C}}}$$

The simplified duty-cycle-to-output transfer function for the flyback power stage operating in DCM is given by:

Ecuacion 49

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where:

$$G_{do} = V_I \times \frac{N_S}{N_P} \times \sqrt{\frac{R \times T_S}{2 \times L_{SEC}}}$$

and

$$\omega_p = \frac{2}{R \times C}$$

3.2.2.5 5 Component Selection

This section presents a discussion of the function of each of the main components of the buck-boost power stage. The electrical requirements and applied stresses are given for each power stage component.

The completed power supply, made up of a power stage and a control circuit, usually must meet a set of minimum performance requirements. This set of requirements is usually referred to as the power supply specification. Many times, the power supply specification determines individual component requirements.

5.1 Output Capacitance

In switching power supply power stages, the output capacitance stores energy in the electric field due to the voltage applied. Thus, qualitatively, the function of a capacitor is to attempt to maintain a constant voltage.

The value of output capacitance of a buck-boost power stage is generally selected to limit output voltage ripple to the level required by the specification. The series impedance of the capacitor and the power stage output current determine the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The following gives guidelines for output capacitor selection.

For continuous inductor current mode operation, to determine the amount of capacitance needed as a function of output load current, *IO*, switching frequency, *fS*, and desired output voltage ripple, ΔVO, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance. This is because the output capacitor supplies the entire output load current during the power stage ON state.

$$C \geq \frac{I_{O(Max)} \times D_{Max}}{f_S \times \Delta V_O}$$

Where IO(Max) is the maximum output current and DMax is the maximum duty cycle.

$$C \geq \frac{I_{O(Max)} \times \left(1 - \sqrt{\frac{2 \times L}{R \times T_S}}\right)}{f_S \times \Delta V_O}$$

For discontinuous inductor current mode operation, to determine the amount of capacitance needed, the following equation is used, assuming all the output voltage ripple is due to the capacitor's capacitance.

However, in many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected.
For continuous inductor current mode operation and assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the ripple to Δ*VO* V peak-to-peak is:

$$ESR \leq \frac{\Delta V_O}{\left(\frac{I_{O(Max)}}{1 - D_{Max}} + \frac{\Delta I_L}{2}\right)}$$

For discontinuous inductor current mode operation and assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the ripple to Δ*VO* V peak-to-peak is simply:

Ecuacion 55

$$ESR \leq \frac{\Delta V_O}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded.
Referring to Figure 3, the output capacitor ripple current is the inductor current, IL, minus the output current, IO. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{C\,RMS} = I_O \times \sqrt{\frac{D}{1 - D}}$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

Three capacitor technologies: low-impedance aluminum, organic semiconductor, and solid tantalum are suitable for low-cost commercial applications.
Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but ESR is higher than the other two. Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds – a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

5.2 Output Inductance

In switching power supply power stages, the function of inductors is to store energy. The energy is stored in their magnetic field due to the current flowing. Thus, qualitatively, the function of an inductor is usually to attempt to maintain a constant current or equivalently to limit the rate of change of current flow.
The value of output inductance of a buck-boost power stage is generally selected to limit the peak-to-peak ripple current flowing in it. In doing so, the power stage's mode of operation, continuous or discontinuous, is determined. The inductor ripple current is directly proportional to the applied voltage and the time that the voltage is applied, and it is inversely proportional to its inductance. This was explained in detail previously.

Many designers prefer to design the inductor themselves, but that topic is beyond the scope of this report. However, the following discusses the considerations necessary for selecting the appropriate inductor. In addition to the inductance, other important factors to be considered when selecting the inductor are its maximum dc or peak current and maximum operating frequency. Using the inductor within its dc current rating is important to insure that it does not overheat or saturate.
Operating the inductor at less than its maximum frequency rating insures that the maximum core loss is not exceeded, resulting in overheating or saturation.
Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them, because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficiently high.

Current flowing through an inductor causes power dissipation due to the inductor's dc resistance; this power dissipation is easily calculated. Power is also dissipated in the inductor's core due to the flux swing caused by the ac voltage applied across it but this information is rarely directly given in manufacturer's data sheets. Occasionally, the inductor's maximum operating frequency and/or applied volt-seconds ratings give the designer some guidance regarding core loss. The power dissipation causes a temperature increase in the inductor. Excessive temperature can cause degradation in the insulation of the winding and cause increased core loss. Care should be exercised to insure all the inductor's maximum ratings are not exceeded.

The loss in the inductor is given by:

Ecuacion 57 $$P_{inductor} = (I_{Lrms})^2 \times R_{Cu} + P_{Core}$$

where, RCu is the winding resistance.

5.3 Power Switch

In switching power supply power stages, the function of the power switch is to control the flow
of energy from the input power source to the output voltage. In a buck-boost power stage, the power switch (Q1 in Figure 1) connects the input to the inductor when the switch is turned on and disconnects when the switch is off. The power switch must conduct the current in the output inductor while on and block the difference between the input voltage and output voltage when off. Also, the power switch must change from one state to the other quickly in order to avoid excessive power dissipation during the switching transition.
The type of power switch considered in this report is a power MOSFET. Other power devices are available but in most instances, the MOSFET is the best choice in terms of cost and performance (when the drive circuits are considered). The two types of MOSFET available for use are the n-channel and the p-channel. P-channel MOSFETs are popular for use in buck-boost power stages because driving the gate is simpler than the gate drive required for an n-channel MOSFET.

The power dissipated by the power switch, Q1, is given by:

$$P_{D(Q1)} = (I_{Lrms})^2 \times R_{DS(on)} \times D + \frac{1}{2} \times (V_I - V_O) \times \left(\frac{I_O}{1-D}\right) \times (t_r + t_f) \times f_S + Q_{Gate} \times V_{GS} \times f_S$$

Where:

t_r and t_f are the MOSFET turn-on and turn-off switching times
Q_{Gate} is the MOSFET total gate charge

Other than selecting p-channel or n-channel, other parameters to consider while selecting the appropriate MOSFET are the maximum drain-to-source breakdown voltage, V(BR)DSS and the maximum drain current, ID(Max).

The MOSFET selected should have a V(BR)DSS rating greater than the maximum difference between the input voltage and output voltage, and some margin should be added for transients and spikes. The MOSFET selected should also have an ID(Max) rating of at least two times the maximum power stage inductor current. However, many times this is not sufficient margin and the MOSFET junction temperature should be calculated to make sure that it is not exceeded. The junction temperature can be estimated as follows:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where:

T_A is the ambient or heatsink temperature $R_{\Theta JA}$ is the thermal resistance from the MOSFET chip to the ambient air or heatsink.

5.4 Output Diode

The output diode conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low-forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low-voltage outputs is usually a Schottky rectifier. The breakdown voltage must be greater than the maximum difference between the input voltage and output voltage, and some margin should be added for transients and spikes. The current rating should be at least two times the maximum power stage output current. Normally the current rating will be much higher than the output current because power and junction temperature limitations dominate the device selection.
The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current. The switching losses which occur at the transitions from conducting to non-conducting states are very small compared to conduction losses and are usually ignored.
The power dissipated by the catch rectifier is given by:

$$P_{D(Diode)} = V_D \times I_O \times (1 - D)$$

where V_D is the forward voltage drop of the catch rectifier.

The junction temperature can be estimated as follows:

$$T_J = T_A + P_D \times R_{\theta JA}$$

3.2.2.6 6 Summary

This application report described and analyzed the operation of the buck-boost power stage. The two modes of operation, continuous conduction mode and discontinuous conduction mode, were examined. Steady-state and small-signal were the two analyses performed on the buck-boost power stage. The flyback power stage was presented as a variation of the basic buck-boost power stage.

The main results of the steady-state analyses are summarized below.

The voltage conversion relationship for CCM is:

Ecuacion 62

$$V_O = -\left[\left(V_I - V_{DS}\right) \times \frac{D}{1-D} - V_d - \frac{I_L \times R_L}{1-D}\right]$$

or a slightly simpler version:

$$V_O = -V_I \times \frac{D}{1-D} \times \frac{1}{1 + \frac{R_L}{R \times (1-D)^2}}$$

which can be simplified to:

$$V_O = -V_I \times \frac{D}{1-D}$$

The relationship between the average inductor current and the output current for the continuous mode buck-boost power stage is given by:

$$I_{L(Avg)} = \frac{-I_O}{(1-D)}$$

The discontinuous conduction mode buck-boost voltage conversion relationship is given by:

$$V_O = -V_I \times \frac{D}{\sqrt{K}}$$

where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

The major results of the small-signal analyses are summarized below.
The small-signal duty-cycle-to-output transfer function for the buck-boost power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = G_{do} \times \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \times \left(1 - \frac{s}{\omega_{z2}}\right)}{1 + \frac{s}{\omega_o \times Q} + \frac{s2}{\omega_o^2}}$$

Where:

$$G_{do} \approx \frac{V_I}{(1 - D)^2}$$

$$s_{z1} = \frac{1}{R_C \times C}$$

$$s_{z2} \approx \frac{(1 - D)^2 \times R}{D \times L}$$

$$\omega_o \approx \frac{1 - D}{\sqrt{L \times C}}$$

$$Q \approx \frac{(1 - D) \times R}{\sqrt{\frac{L}{C}}}$$

The small-signal duty-cycle-to-output transfer function for the buck-boost power stage operating in DCM is given by:

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where:

$$G_{do} = \frac{V_O}{D} = -\frac{V_I}{\sqrt{K}}$$

Ecuacion 71

$$\omega_p = \frac{2}{R \times C}$$

Also presented were requirements for the buck-boost power stage components based on voltage and current stresses applied during the operation of the buck-boost power stage. For further study, several references are given.

3.2.2.7 7 References

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2	Application Report *Designing Fast Response Synchronous Buck Regulators Using theTPS5210*	TI Literature Number SLVA044
3. V. Vorperian, R. Tymerski, and F. C. Lee	*Equivalent Circuit Models for Resonant and PWM Switches*, *IEEE*	*Transactions on Power Electronics*, Vol. 4, No. 2, pp. 205-214, April 1989.
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3.2.3 Choosing Inductors and Capacitors for DC/DC Converters

BY: Christophe Vaucourt

ABSTRACT
Wireless handsets, PDAs, and other portable electronic devices continue to shrink while ncreasing in complexity. As a result, engineers face design challenges with battery life, PC-board space, and power dissipation. These problems can be overcome by increasing the efficiency of the dc/dc converters used in these products. Efficiency is often the primary design goal when using a dc/dc converter. Many design requirements involve converting the battery voltage to a low supply voltage. Although a linear regulator can be used, it cannot achieve the efficiency of a switching-regulator design. This article covers some of the common issues designers face when balancing circuit size, performance, and cost.

3.2.3.1 Large-Signal vs Small-Signal Response

Switching converters employ complex regulation schemes to keep efficiency high at both heavy and light loads. Modern CPUs require fast large-signal response from the regulator. For instance, when a processor is switching from idle to full-speed operation, the current drawn by the core can quickly rise from a few tens of micro amps to hundreds of milliamps.

As load conditions change, the control loop rapidly responds to the new requirements in order to keep the voltage within the regulation limits. The amount and rate of load change determines whether the loop response is called a large-signal response or a small-signal response. We define the small-signal parameters based on a steady-state operating point. Consequently, we can typically consider variations below 10% of a steady-state operating point as being a small signal variation.

In practice, when a load demands a sudden current increase, the error amplifier is in slew limit and does not control the loop. This is because the load transient occurs faster than the error amplifier can respond, so the output capacitors satisfy the transient current until the inductor current can catch up.

Large-signal response temporarily takes the loop out of operation. However, the loop must respond smoothly going into and out of large-signal response. The wider the loop bandwidth, thefaster the load transient the loop can respond to.

Even though the regulation loop, from a small-signal prospective, may show enough gain and phase margin, the switching converter can still exhibit instability and ringing during line or load transients. When selecting external components, power supply designers need to be aware of these limitations, otherwise their designs could fail in practical use.

3.2.3.2 Inductor Selection

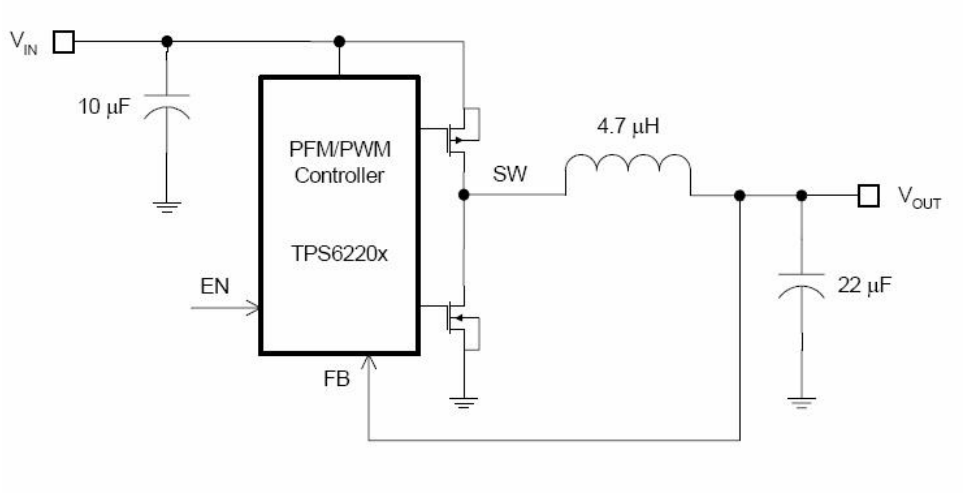

Figure 1. Basic Buck Regulator

The basic buck-regulator circuit shown in Figure 1 is used for the discussion of inductor selection. For most TPS6220x applications, the inductor value ranges from 4.7 µH to 10 µH. Its value is chosen based on the desired ripple current. Usually, it is recommended to operate the circuit with a ripple current of less than 20% of the average inductor current. Higher VIN or VOUT also increases the ripple current as shown in Equation 1. The inductor must be able to handle the peak switching current without saturating the core, which would result in a loss of inductance.

EQUATION (1)

$$\Delta I_L = \frac{1}{f * L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

At the expense of higher output-voltage ripple, small-value inductors result in a higher outputcurrent slew rate, improving the load transient response of the converter. Large-value inductors lower the ripple current and reduce the core magnetic hysteresis losses.

The total coil losses can be combined into the loss resistance (RS), which is effectively connected in series with the ideal inductance (LS). This results in the simplified equivalent circuit shown in Figure 2.

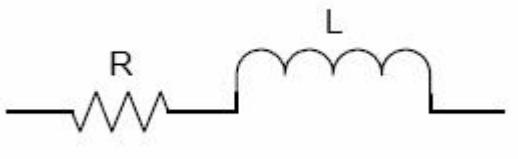

Figure 2. Inductor Simplified Equivalent Circuit

Even though the losses in RS are frequency dependent, the dc resistance (Rdc) is also specified in inductor data sheets. This depends on the wire material and size, and the construction type of SMD inductors. It is characterized at room temperature by a simple resistance measurement.
The size of Rdc directly influences temperature rises in the coil. Prolonged operation above the current rating must be avoided.
The total coil losses consist of both the losses due to Rdc, and the following frequency dependent components:
• Core-material losses (magnetic hysteresis loss, eddy-current loss)
• Skin-effect losses in the conductor (current displacement at high frequencies)
• Magnetic-field losses of adjacent windings (proximity effect)
• Radiation losses

All these loss components can be combined into a series RS. This loss resistance is primarily responsible for defining the quality of the inductor. Unfortunately, mathematical determination of RS is impractical. Therefore, inductors are usually measured over the entire frequency range with an impedance analyzer. This measurement provides the individual components XL(f), RS(f) and Z(f).
The ratio of reactance (XL) to total resistance (RS) of an induction coil is known as the quality factor Q, see Equation 2. Q is defined as a quality characteristic of the inductor. The larger the losses are, the poorer the inductor acts as an energy storage element.

$$Q = \frac{X_L}{R_S} = \frac{\omega L}{R_S} = \frac{\text{Reactance}}{\text{Total Resistance}}$$

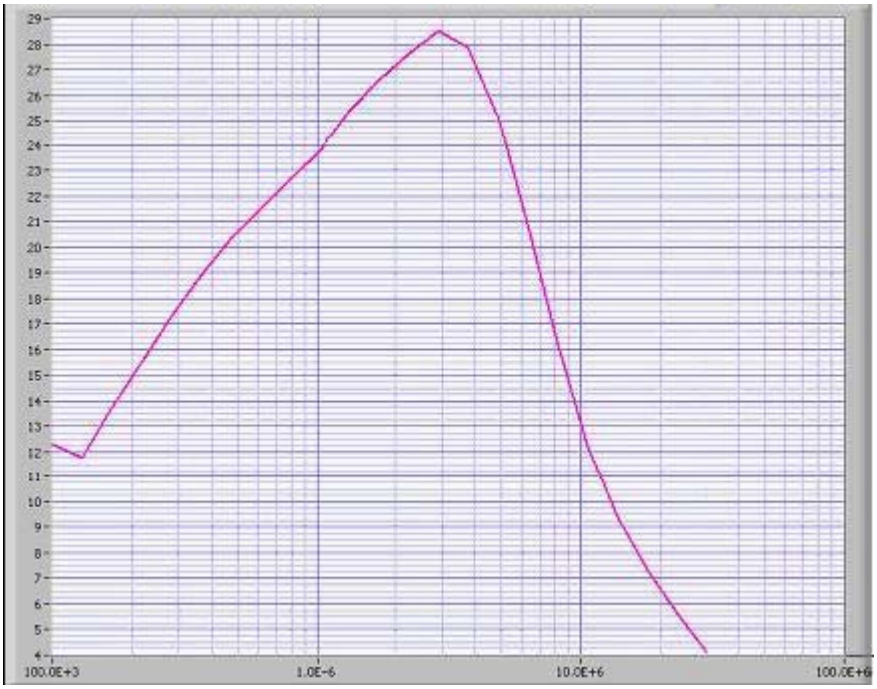

Figure 3. Q vs Frequency (Hz)

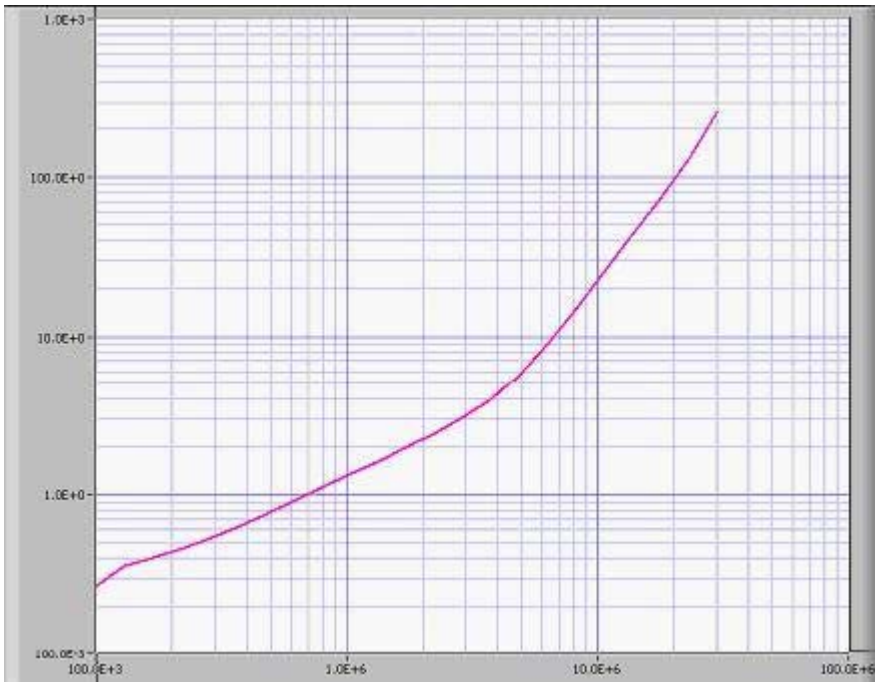

Figure 4. RS (Ω) vs Frequency (Hz) 4.7-µH wire wound inductor, Rdc = 240 mΩ, ISAT = 700 mA

The quality-frequency graph is helpful in selecting the best inductor construction for the particular application. As it appears on the measurement results in Figure 3, the operating range with the smallest losses (highest Q) can be defined up to the quality turning point. If the inductor is used at higher frequencies, the losses increase rapidly, and Q decreases.
A properly designed inductor degrades efficiency by only a small percentage. Different core materials and shapes change the size/current and price/current relationship of an inductor.
Shielded inductors in ferrite material are small and don't radiate much energy. Choosing an inductor often depends on the price/size tradeoffs, and on requirements for radiatedfield/ electromagnetic-interference suppression.

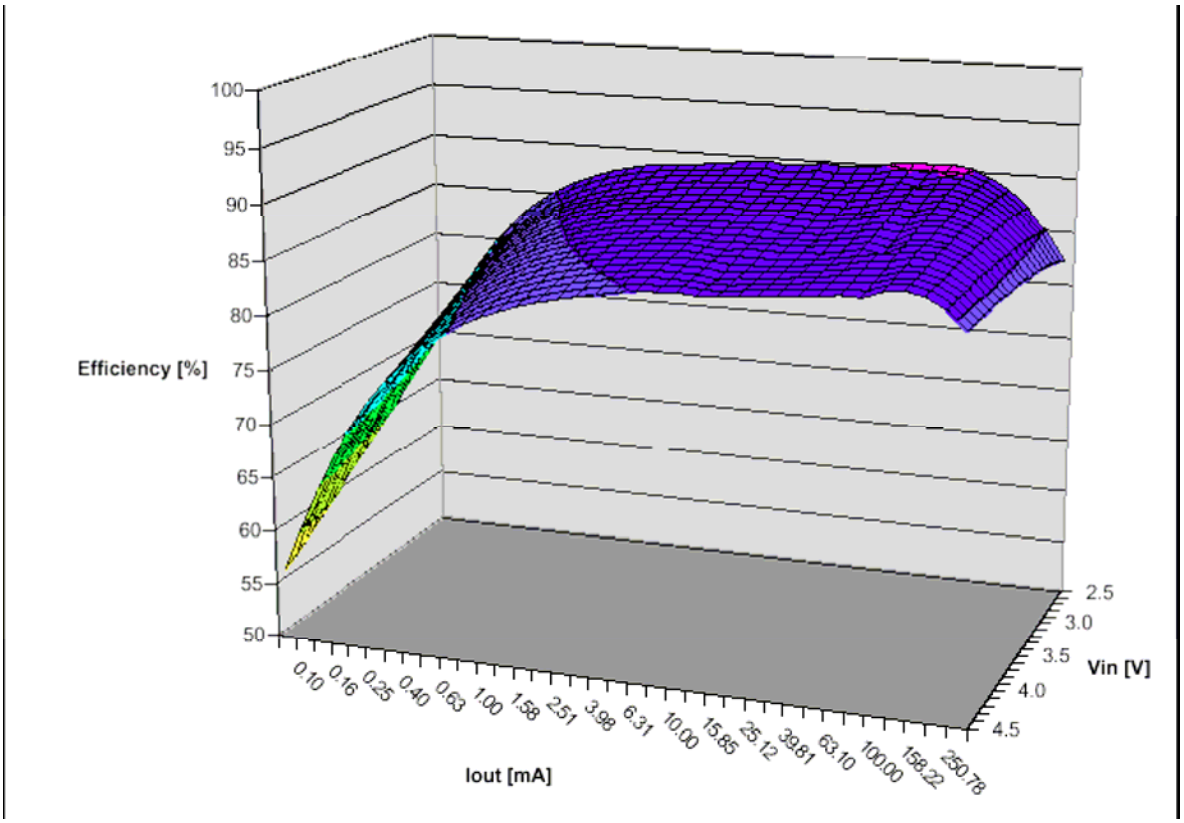

Figure 5. TPS62204 (1.6V) Efficiency vs Load Current vs Input Voltage With 4.7-µH Wire-Wound Inductor, Rdc = 240 mΩ / ISAT = 700 mA

3.2.3.3 Output Capacitor

The designer can downsize the output capacitor to save money and board space. The basic selection of the output capacitor is based on the ripple current and ripple voltage, as well as on loop stability considerations.

The effective series resistance (ESR) of the output capacitor and the inductor value directly affect the output ripple voltage. The output ripple voltage can easily be estimated based on the inductor ripple current (ΔIL) and output capacitor ESR. Therefore, a capacitor with the lowest possible ESR is recommended. For example, 4.7- to 10-µF capacitors in X5R/X7R technology have ESR values of approximately 10 mΩ. Smaller capacitors are acceptable for light loads, or in applications where ripple is not a concern. The control-loop architecture developed by Texas Instruments allows the designer to choose the output capacitors and externally compensate the control loop for optimum transient response and loop stability. Of course, the internal compensation works best with one set of operating conditions and is sensitive to output capacitor characteristics.

The TPS6220x-series step-down converters have internal loop compensation. Therefore, the external L-C filter must be compatible with the internal compensation. For this device, the internal compensation is optimized for an LC corner frequency of 16 kHz, i.e., a 10-µH inductor and 10-µF output capacitor. As a general rule of thumb, the product of L*C should not vary over a wide range when selecting an output filter. This is especially important when selecting smaller inductor or capacitor values that move the corner frequency to higher frequencies.

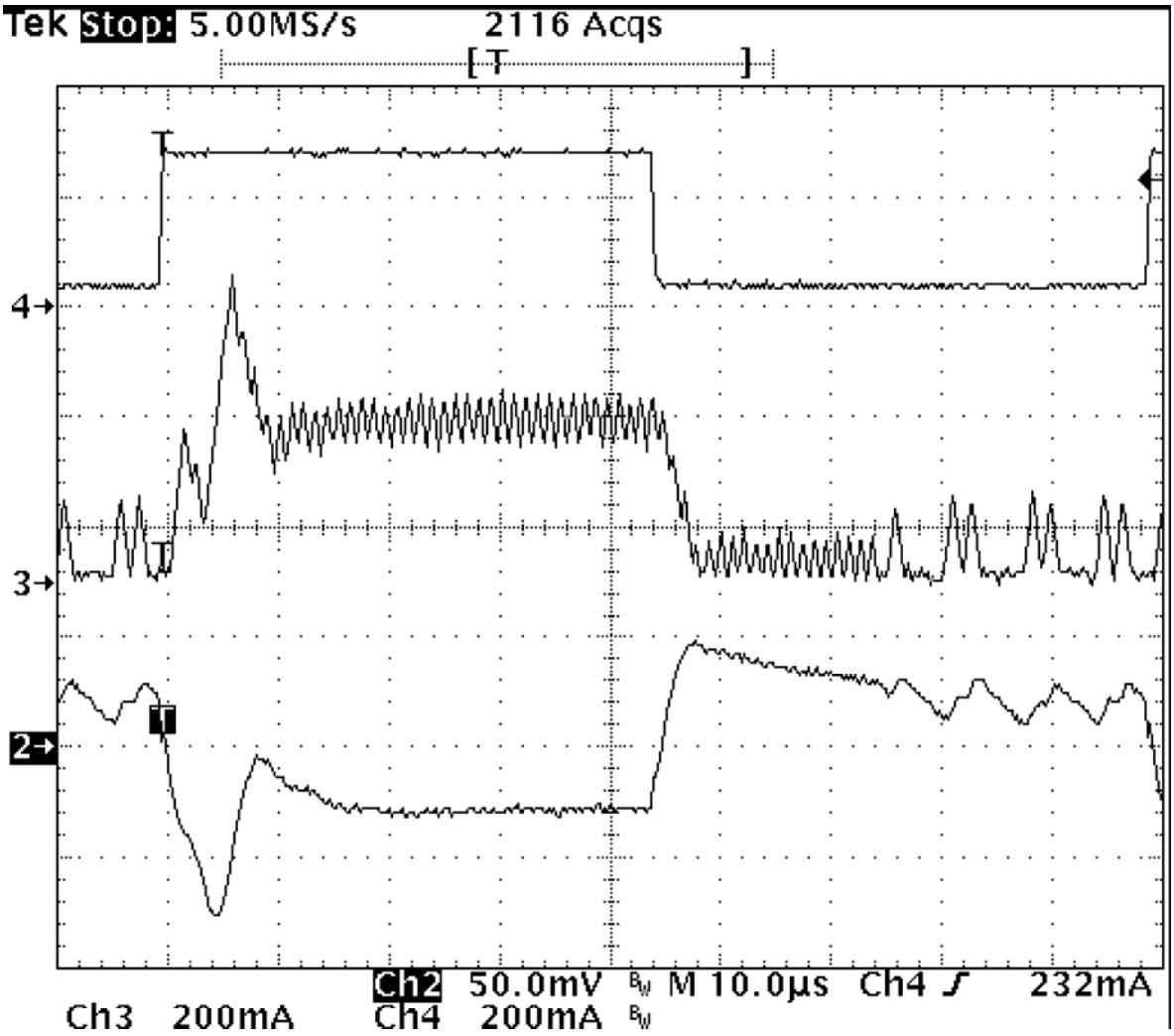

Figure 6. L = 10 µH / COUT = 10 µF

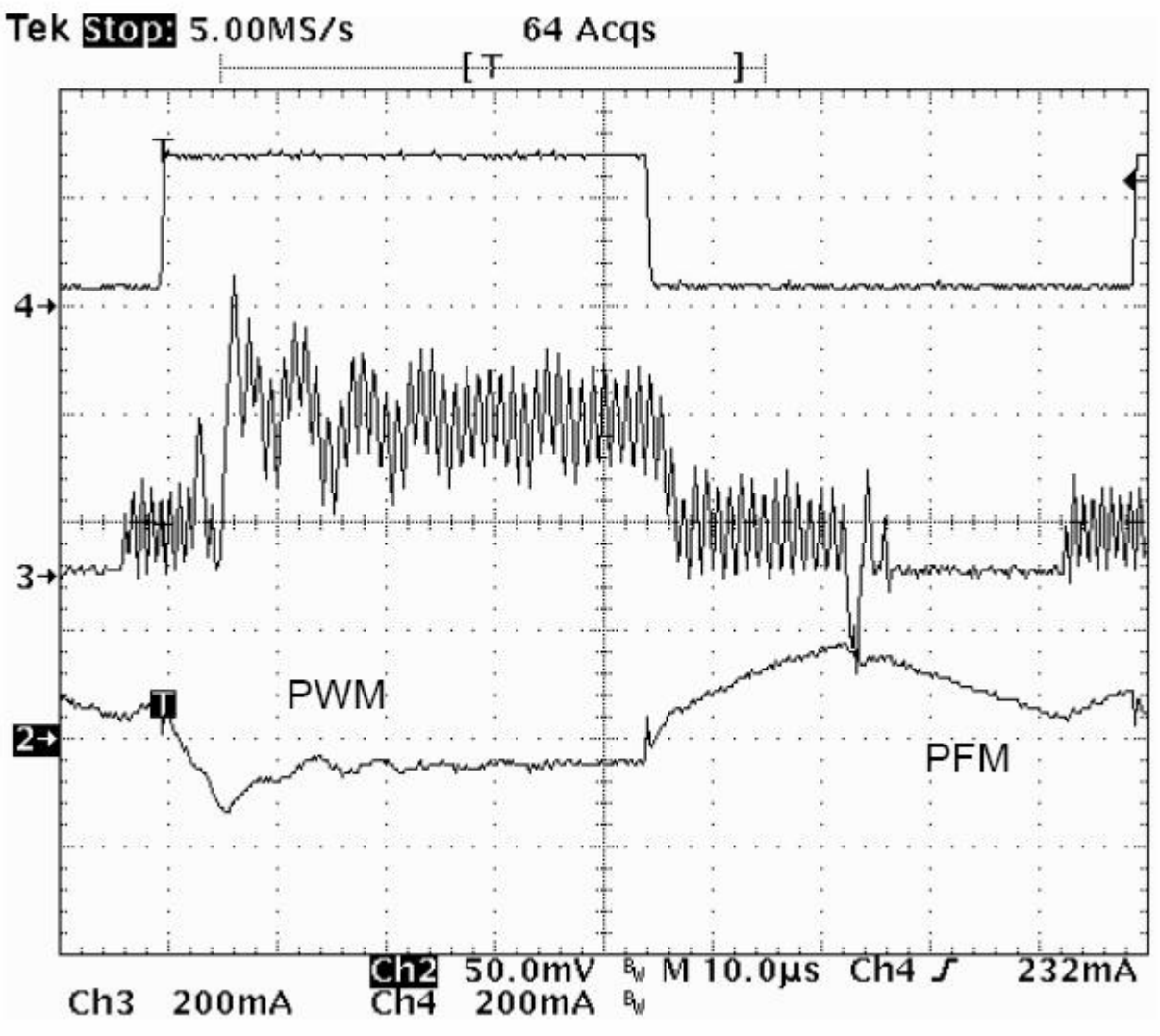

Figure 7. L = 4.7 µH / COUT = 22 µF

TPS62204 load transient performance vs L-C filter combination
3.6-V input voltage / 1.6-V fixed output voltage

3.2.3.4 References

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3.3 Etapas entrada-salida. (2.3)

3.4 Circuiteria de control. (2.4)

3.5 Circuiteria de protección y auxiliar. (2.5)

3.5.1 Transient Suppression Devices and Principles

Application Note January 1998 AN9768

3.5.1.1 Transient Suppression Devices

There are two major categories of transient suppressors: a) those that attenuate transients, thus preventing their propagation into the sensitive circuit; and b) those that divert transients away from sensitive loads and so limit the residual voltages.

Attenuating a transient, that is, keeping it from propagating away from its source or keeping it from impinging on a sensitive load is accomplished with filters inserted in series within a circuit. The filter, generally of the low-pass type, attenuates the transient (high frequency) and allows the signal or power flow (low-frequency) to continue undisturbed.

Diverting a transient can be accomplished with a voltage-clamping type device or with a "crowbar" type device. The designs of these two types, as well as their operation and application, are different enough to warrant a brief discussion of each in general terms. A more detailed description will follow later in this section.

A voltage-clamping device is a component having a variable impedance depending on the current flowing through the device or on the voltage across its terminal. These devices exhibit a nonlinear impedance characteristic that is, Ohm's law is applicable but the equation has a variable R. The variation of the impedance is monotonic; in other words, it does not contain discontinuities in contrast to the crowbar device, which exhibits a turn-on action. The volt-ampere characteristic of these clamping devices is somewhat time-dependent, but they do not involve a time delay as do the sparkover of a gap or the triggering of a thyristor. With a voltage-clamping device, the circuit is essentially unaffected by the presence of the device before and after the transient for any steady-state voltage below the clamping level. The voltage clamping action results from the increased current drawn through the device as the voltage tends to rise. If this current increase is greater than the voltage rise, the impedance of the device is nonlinear (Figure 1). The apparent "clamping" of the voltage results from the increased voltage drop (IR) in the source impedance due to the increased current. It should be clearly understood that the device depends on the source impedance to produce the clamping. One is seeing a voltage divider action at work, where the ratio of the divider is not constant but changes.

However, if the source impedance is very low, then the ratio is low. The suppressor cannot be effective with zero source impedance (Figure 2) and works best when the voltage divider action can be implemented.

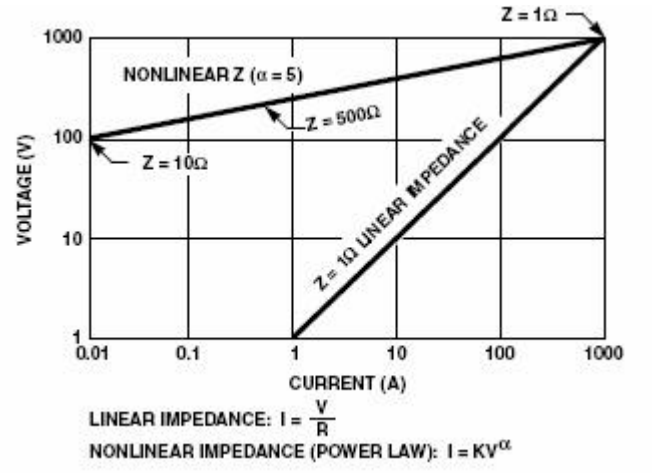


FIGURE 1. VOLTAGE/CURRENT CHARACTERISTIC FOR A LINEAR 1Ω RESISTOR AND NONLINEAR

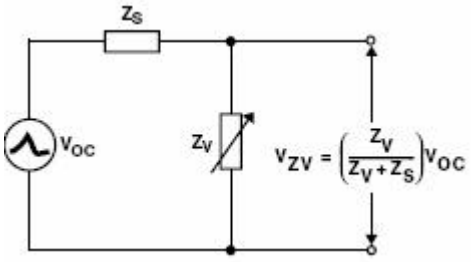


FIGURE 2A. VOLTAGE CLAMPING DEVICE

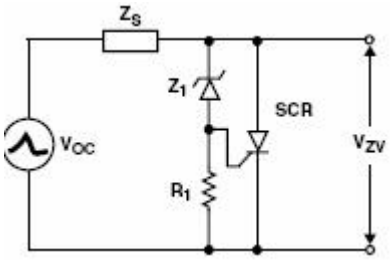


FIGURE 2B. CROWBAR DEVICE

FIGURE 2. DIVISION OF VOLTAGE WITH VARIABLE IMPEDANCE SUPPRESSOR

Crowbar-type devices involve a switching action, either the breakdown of a gas between electrodes or the turn-on of a thyristor, for example. After switching on, they offer a very low impedance path which diverts the transient away from the parallel-connected load.
These types of crowbar devices can have two limitations. One is delay time, which could leave the load unprotected during the initial transient rise. The second is that a power current from the voltage source will follow the surge discharge (called "follow-current" or "power-follow"). In AC circuits, this power-follow current may not be cleared at a natural current zero unless the device is designed to do so; in DC circuits the clearing is even more uncertain. In some cases, additional means must be provided to "open" the crowbar.

3.5.1.2 Filters

The frequency components of a transient are several orders of magnitude above the power frequency of an AC circuit and, of course, a DC circuit. Therefore, an obvious solution is to install a low-pass filter between the source of transients and the sensitive load. The simplest form of filter is a capacitor placed across the line. The impedance of the capacitor forms a voltage divider with the source impedance, resulting in attenuation of the transient at high frequencies. This simple approach may have undesirable side effects, such as a) unwanted resonances with inductive components located elsewhere in the circuit leading to high peak voltages; b) high inrush currents during switching, or, c) excessive reactive load on the power system voltage. These undesirable effects can be reduced by adding a series resistor hence, the very popular use of RC snubbers and suppression networks. However, the price of the added resistance is less effective clamping. Beyond the simple RC network, conventional filters comprising inductances and capacitors are widely used for interference protection. As a bonus, they also offer an effective transient protection, provided that the filter's frontend components can withstand the high voltage associated with the transient. There is a fundamental limitation in the use of capacitors and filters for transient protection when the source of transients in unknown. The capacitor response is indeed nonlinear with frequency, but it is still a linear function of current.

To design a protection scheme against random transients, it is often necessary to make an assumption about the characteristics of the impinging transient. If an error in the source impedance or in the open-circuit voltage is made in that assumption, the consequences for a linear suppressor and a nonlinear suppressor are dramatically different as demonstrated by the following comparison.

A Simplified Comparison Between Protection with Linear and Nonlinear Suppressor Devices

Assume an open-circuit voltage of 3000V (see Figure 2):

1. If the source impedance is Z S= 50Ω
With a suppressor impedance of ZV=8Ω

The expected current is:

1 = 3000 / 50 + 8 = 51.7A and VR= 8 X 51.7 = 414V

The maximum voltage appearing across the terminals of a typical nonlinear V130LA20A varistor at 51.7A is 330V.
Note that:

ZS X I=	50 X 51.7	=	2586V
ZV X I=	8 X 51.7 =	414V	
	=	3000V	

2. If the source impedance is only 5Ω
(a 10:1 error in the assumption), the voltage across the same linear 8Ω suppressor is:

VR = 3000 8/ 5+8 = 1850V

However, the nonlinear varistor has a much lower impedance; again, by iteration from the characteristic curve, try 400V at 500A, which is correct for the V130LA20A; to prove the correctness of our "educated guess" we calculate I,

I = 3000-400V / = 5 = 520A

ZS x I = 5 x 520	=	2600V
VC =		400
	=	3000V

which justifies the "educated guess" of 500A in the circuit.

Summary

Similar calculations can be made, with similar conclusions, for an assumed error in open-circuit voltage at a fixed source impedance. In that case, the linear device is even more sensitive to an error in the assumption. The calculations are left for the interested reader to work out.

The example calculated in the simplified comparison between protection with linear and nonlinear suppression devices shows that a source impedance change from an assumed 50 Ω to 5 Ω can produce a change of about 414V to 1850V for the protective voltage of a typical linear suppressor. With a typical nonlinear suppressor, the

TABLE 1. 3000V "OPEN-CIRCUIT" TRANSIENT VOLTAGE

PROTECTIVE DEVICE	ASSUMED SOURCE IMPEDANCE	
	50 Ω	**5** Ω
	PROTECTIVE LEVEL ACHIEVED	
Linear 8 Ω	414V	1850V
Nonlinear Varistor	330V	400V

corresponding change is only 330V to 400V. In other words, a variation of only 21% in the protective level achieved with a nonlinear suppressor occurs for a 10 to 1 error in the assumption made on the transient parameters, in contrast to a 447% variation in the protective level with a linear suppressor for the same error in assumption. Nonlinear voltage-clamping devices give the lowest clamping voltage, resulting in the best protection against transients.

3.5.1.3 Crowbar Devices

This category of suppressors, primarily gas tubes or carbonblock protectors, is widely used in the communication field where power-follow current is less of a problem than in power circuits. Another form of these suppressors is the hybrid circuit which uses solid-state or MOV devices. In effect, a crowbar device short-circuits a high voltage to ground. This short will continue until the current is brought to a low level. Because the voltage (arc or forward-drop) during the discharge is held very low, substantial currents can be carried by the suppressor without dissipating a considerable amount of energy within it. This capability is a major advantage. Volt-Time Response - When the voltage rises across a spark gap, no significant conduction can take place until transition to the arc mode has occurred by avalanche breakdown of the gas between the electrodes. Power-Follow - The second characteristic is that a power current from the steady-state voltage source will follow the surge discharge (called "follow-current" or "power-follow").

3.5.1.4 Voltage-Clamping Devices

To perform the voltage limiting function, voltage-clamping devices at the beginning of the section depend on their nonlinear impedance in conjunction with the transient source impedance. Three types of devices have been used: reverse selenium rectifiers, avalanche (Zener) diodes and varistors made of different materials, i.e., silicon carbide, zinc oxide, etc. [1].

3.5.1.5 Selenium Cells -

Selenium transient suppressors apply the technology of selenium rectifiers in conjunction with a special process allowing reverse breakdown current at highenergy levels without damage to the polycrystalline structure. These cells are built by developing the rectifier elements on the surface of a metal plate substrate which gives them good thermal mass and energy dissipation performance. Some of these have self-healing characteristics which allows the device to survive energy discharges in excess of the rated values for a limited number of operations characteristics that are useful, if not "legal" in the unsure world of voltage transients.

The selenium cells, however, do not have the clamping ability of the more modern metal-oxide varistors or avalanche diodes. Consequently, their field of application has been considerably diminished.

3.5.1.6 Zener Diodes -

Silicon rectifier technology, designed for transient suppression, has improved the performance of regulator-type Zener diodes. The major advantage of these diodes is their very effective clamping, which comes closest to an ideal constant voltage clamp. Since the diode maintains the avalanche voltage across a thin junction area during surge discharge, substantial heat is generated in a small volume. The major limitation of this type of device is its energy dissipation capability.

3.5.1.7 Silicon Carbide Varistors -

Until the introduction of metaloxide varistors, the most common type of "varistor" was made from specially processed silicon carbide. This material was very successfully applied in high-power, high-voltage surge arresters. However, the relatively low a values of this material produce one of two results. Either the protective level is too high for a device capable of withstanding line voltage or, for a device producing an acceptable protective level, excessive standby current would be drawn at normal voltage if directly connected across the line. Therefore, a series gap is required to block the normal voltage. In lower voltage electronic circuits, silicon carbide varistors have not been widely used because of the need for using a series gap, which increases the total cost and reproducessome of the characteristics of gaps described earlier. However, this varistor has been used as a current-limiting resistor to assist some gaps in clearing power-follow current.

3.5.1.8 Metal-Oxide Varistors -

A varistor functions as a nonlinear variable impedance. The relationship between the current in the device, I , and the voltage across the terminals, V is typically described by a power law: $I = kV^{\alpha}$. While more accurate and more complete equations can be derived to reflect the physics of the device, [2, 3] this definition will suffice here. A more detailed discussion will be found in Application Note AN9767, "Littelfuse Varistors – Basic Properties, Terminology and Theory". The term α (alpha) in the equation represents the degree of nonlinearity of the conduction. A linear resistance has an α = 1. The higher the value of a, the better the clamp, which explains why α is sometimes used as a figure of merit. Quite naturally, varistor manufacturers are constantly striving for higher alphas. This family of transient voltage suppressors are made of sintered metal oxides, primarily zinc oxide with suitable additives. These varistors have α values considerably greater than those of silicon carbide varistors, typically in the range of an effective value of 15 to 30 measured over several decades of surge current. The high exponent values (α) of the metal-oxide varistors have opened completely new fields of applications by providing a sufficiently low protective level and a low standby current. The opportunities for applications extend from lowpower electronics to the largest utility-type surge arresters.

3.5.1.9 Transient Suppressors Compared

Because of diversity of characteristics and nonstandardized manufacturer specifications, transient suppressors are not easy to compare. A graph (Figure 3) shows the relative voltampere characteristics of the four common devices that are used in 120V AC circuits. A curve for a simple ohmic resistor is included for comparison. It can be seen that as the alpha factor increases, the curve's voltage-current slope becomes less steep and approaches an almost constant voltage. High alphas are desirable for clamping applications that require operation over a wide range of currents. It also is necessary to know the device energy-absorption and peak-current capabilities when comparisons are made. Table 2 includes other important parameters of commonly used suppressors.

3.5.1.10 Standby Power -

The power consumed by the suppressor unit at normal line voltage is an important selection criterion. Peak standby current is one factor that determines the standby power of a suppressor. The standby power dissipation depends also on the alpha characteristic of the device.

As an example, a selenium suppressor in Table 2 can have a 12mA peak standby current and an alpha of 8 (Figure 3). Therefore, it has a standby power dissipation of about 0.5W on a 120V RMS line (170V peak). A zener-diode suppressor has standby power dissipation of less than a milliwatt. And a silicon-carbide varistor, in a 0.75" diameter disc, has standby power in the 200mW range. High standby power in the lower alpha devices is necessary to achieve a reasonable clamping voltage at higher currents.

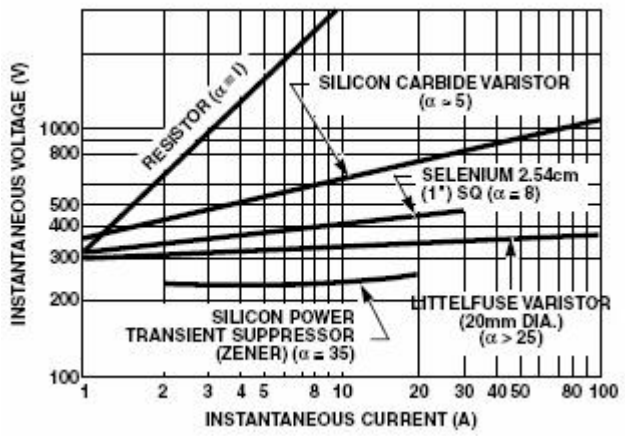
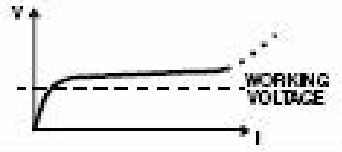
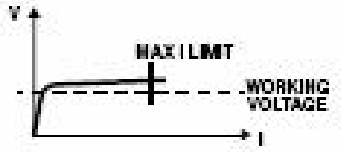
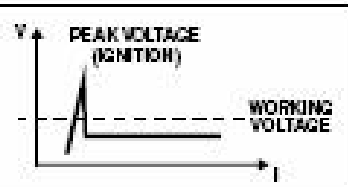
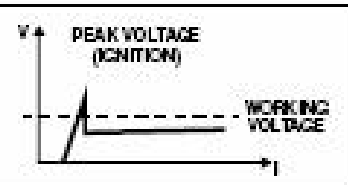
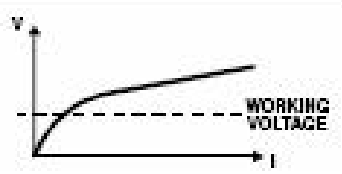
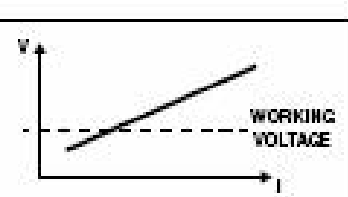


FIGURE 3. V-I CHARACTERISTIC OF FOUR TRANSIENT SUPPRESSOR DEVICE

TABLE 2. CHARACTERISTICS AND FEATURES OF TRANSIENT VOLTAGE SUPPRESSOR TECHNOLOGY

V-I CHARACTERISTICS	DEVICE TYPE	LEAK-AGE	FOLLOW ON I	CLAMPING VOLTAGE	ENERGY CAPABIL-ITY	CAPACI-TANCE	RE-SPONSE TIME	COST
	Ideal Device	Zero To Low	No	Low	High	Low Or High	Fast	Low
	Zinc Oxide Varistor	Low	No	Moderate To Low	High	Moderate To High	Fast	Low
	Zener	Low	No	Low	Low	Low	Fast	High
	Crowbar (Zener - SCR Combination)	Low	Yes (Latching Holding I)	Low	Medium	Low	Fast	Moderate
	Spark Gap	Zero	Yes	High Ignition Voltage Low Clamp	High	Low	Slow	Low To High
	Triggered Spark Gap	Zero	Yes	Lower Ignition Voltage Low Clamp	High	Low	Moderate	Moderate
	Selenium	Very High	No	Moderate To High	Moderate To High	High	Fast	High
	Silicon Carbide Varistor	High	No	High	High	High	Fast	Low

The amount of standby power that a circuit can tolerate may be the deciding factor in the choice of a suppressor. Though high-alpha devices have low standby power at the nominal design voltage, a small line-voltage rise would cause a dramatic increase in the standby power. Figure 4 shows that for a zener-diode suppressor, a 10% increase above rated voltage increases the standby power dissipation above its rating by a factor of 30. But for a low-alpha device, such as silicon carbide, the standby power increases by only 1.5 times.
Typical volt-time curves of a gas discharge device are shown in Figure 5 indicating an initial high clamping voltage. The gas-discharge suppressor turns on when the transient pulse exceeds the impulse sparkover voltage. Two representative surge rates 1kV/ µs and 20kV/µs are shown in Figure 5. When a surge voltage is applied, the device turns on at some point within the indicated limits. At 20kV/µs, the discharge unit will sparkover between 600V and 2500V. At 1kV/µs, it will sparkover between 390V and 1500V.

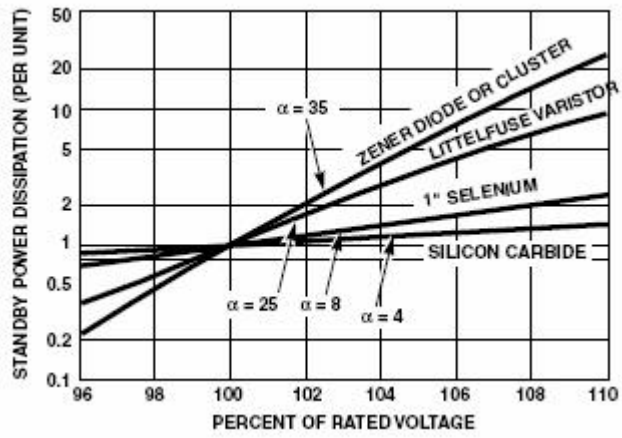


FIGURE 4. CHANGES IN STANDBY POWER ARE CONSIDERABLY GREATER WHEN THE SUPPRESSOR'S ALPHA IS HIGH

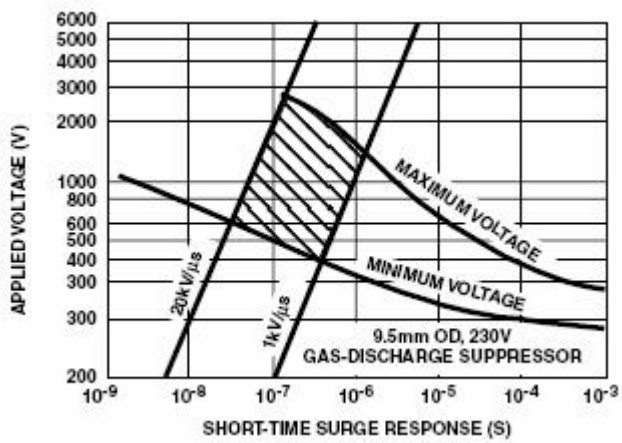


FIGURE 5. IMPULSE BREAKOVER OF A GAS-DISCHARGE DEVICE DEPENDS UPON THE RATE OF VOLTAGE RISE AS WELL AS THE ABSOLUTE VOLTAGE LEVEL

The gas discharge device may experience follow-current. As the AC voltage passes through zero at the end of every half cycle the arc will extinguish, but if the electrodes are hot and the gas is ionized, it may reignite on the next cycle.
Depending on the power source, this current may be sufficient to cause damage to the electrodes. The follow current can be reduced by placing a limiting resistor in series with the device, or, selecting a GDT specifically designed for this application with a high follow-current threshold. The gas discharge device is useful for high current surges and it is often advantageous to provide another suppression device in a combination that allows the added suppressor to protect against the high initial impulse. Several hybrid combinations with a varistor or avalanche diode are possible.

3.5.1.11 Comparison of Peak Pulse Power.

Zener Diode and Littelfuse Varistor Transient Suppressors

Transient suppressors have to be optimized to absorb large amounts of power or energy in a short time duration: nanoseconds, microseconds, or milliseconds in some instances.
Electrical energy is transformed into heat and has to be distributed instantaneously throughout the device. Transient thermal impedance is much more important than steady state thermal impedance, as it keeps peak junction temperature to a minimum. In other words, heat should be instantly and evenly distributed throughout the device.
The varistor meets these requirements: an extremely reliable device with large overload capability. Zener diodes dissipate electrical energy into heat in the depletion region of the die, resulting in high peak temperature.
Figure 6 shows Peak Pulse Power vs Pulse width for the V8ZA2 and the P6KE 6.8, the same devices compared for leakage current.
At 1ms, the two devices are almost the same. At 2 µs the varistor is almost 10 times greater, 7kW for the P6KE 6.8 Zener vs 60kW for the varistor V8ZA2.

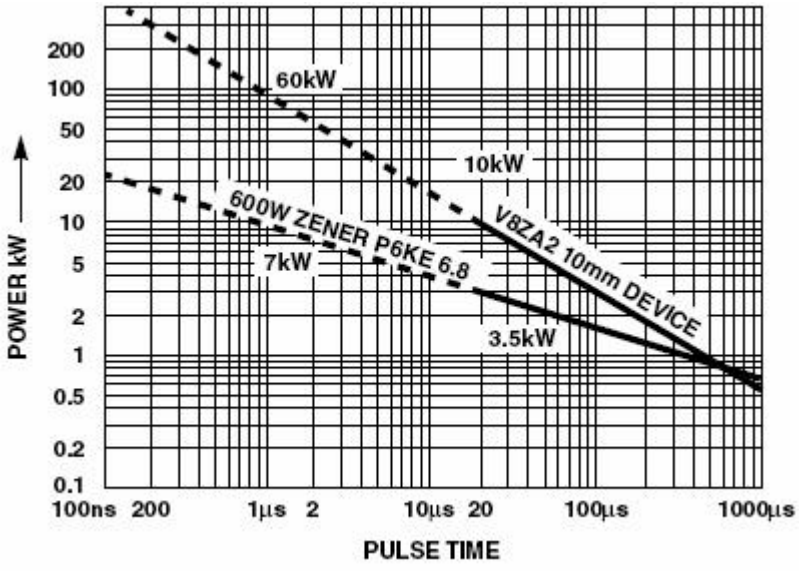


FIGURE 6. PEAK PULSE POWER vs PULSE TIME

3.5.1.11.1 Clamping Voltage

Clamping voltage is an important feature of a transient suppressor. Zener diode type devices have lower clamping voltages than varistors. Because these protective devices are connected in parallel with the device or system to be protected, a lower clamping voltage can be advantageous in certain applications.

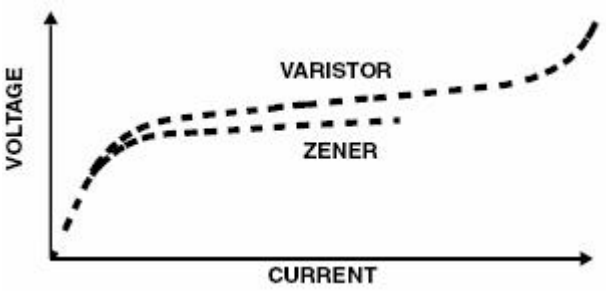


FIGURE 7. CHARACTERISTICS OF ZENER AND VARISTOR

3.5.1.11.2 Speed of Response

Response times of less than 1ps are sometimes claimed for zener diodes, but these claims are not supported by data in practical applications. For the varistor, measurements were made down to 500ps with a voltage rise time (dv/dt) of 1 million volts per microsecond. These measurements are described in Application Note AN9767. Another consideration is the lead effect. Detailed information on the lead effect can be found further in this section and in Application Note AN9773. In summary, both devices are fast enough to respond to real world transient events.

3.5.1.11.3 Leakage Current

Leakage current can be an area of misconception when comparing a varistor and zener diode, for example. Figure 8 shows a P6KE 6.8 and a V8ZA2, both recommended by their manufacturers for protection of integrated circuits having 5V supply voltages**.**
The zener diode leakage is about 100 times higher at 5V than the varistor, 200 µA vs less than 2 µA, in this example.

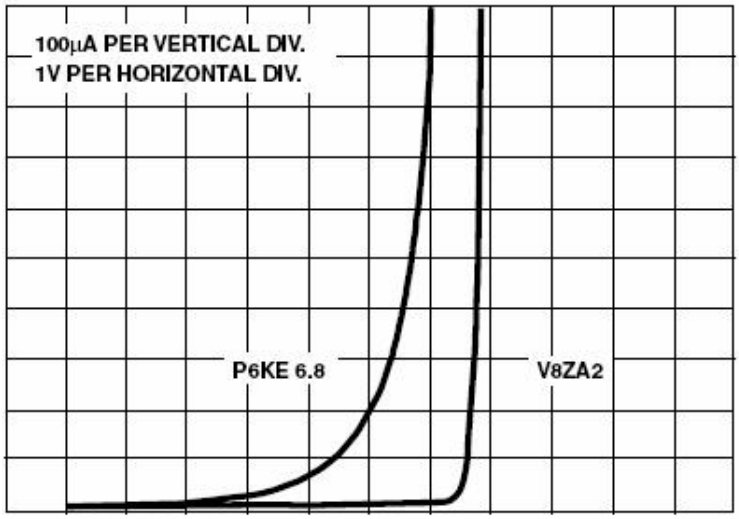


FIGURE 8. CHARACTERISTIC OF ZENER P6KE 6.8 vs LITTELFUSE VARISTOR V8ZA2

The leakage current of a zener can be reduced by specifying a higher voltage device.

3.5.1.11.4 "Aging"

It has been stated that a varistor's V-I characteristic changes every time high surge current or energy is subjected to it. That is not the case. As illustrated in Figure 9, the V-I characteristic initially changed on some of the devices, but returned to within a few percent of its original value after applying a second or third pulse. To be conservative, peak pulse limits have been established on data sheets. In many cases, these limits have been exceeded many fold without harm to the device. This does not mean that established limits should be exceeded, but rather, viewed in perspective of the definition of a failed device. A "failed" varistor device shows a ± 10% change of the V-I characteristic at the 1mA point.

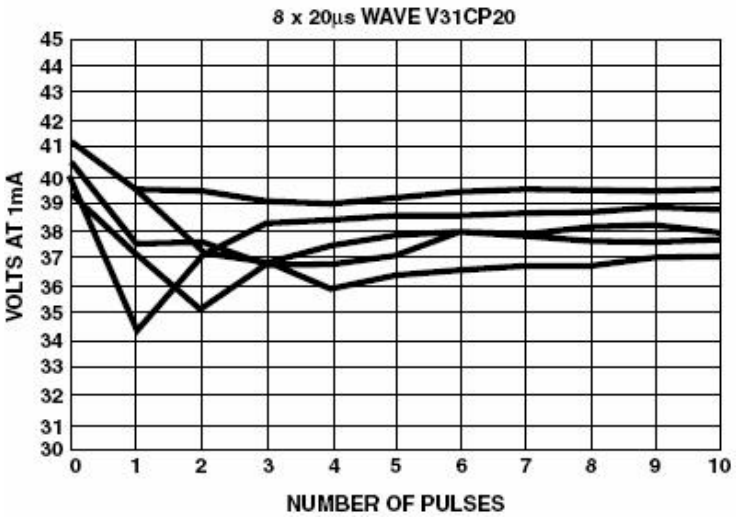


FIGURE 9. 250A PULSE WITHSTAND CAPABILITIES

3.5.1.11.5 Failure Mode

Varistors subjected to energy levels beyond specified ratings may be damaged. Varistors fail in the short circuit mode. Subjected to high enough energy, however, they may physically rupture or explode, resulting in an open circuit condition. These types of failures are quite rare for properly selected devices because of the large peak pulse capabilities inherent in varistors. Zeners can fail either short or open. If the die is connected by a wire, it can act as a fuse, disconnecting the device and resulting in an Open circuit. Designers must analyze which failure mode, open or short, is preferred for their circuits. When a device fails during a transient, a short is preferred, as it will provide a current path bypassing and will continue to protect the sensitive components. On the other hand, if a device fails open during a transient, the remaining energy ends up in the sensitive components that were supposed to be protected. Another consideration is a hybrid approach, making use of the best features of both types of transient suppressors (See Figure 10).

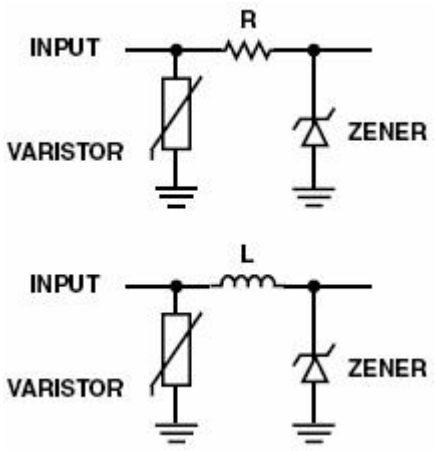


FIGURE 10. HYBRID PROTECTION USING VARISTORS, ZENERS, R AND L

3.5.1.11.6 Capacitance

Depending on the application, transient suppressor capacitance can be a very desirable or undesirable feature. Varistors in comparison to zener diodes have a higher capacitance. In DC circuits capacitance is desirable, the larger the better. Decoupling capacitors are used on IC supply voltage pins and can in many cases be replaced by varistors, providing both the decoupling and transient voltage clamping functions. The same is true for filter connectors where the varistor can perform the dual functions of providing both filtering and transient suppression. There are circuits however, where capacitance is less desirable, such as high frequency digital or some analog circuits.

As a rule the source impedance of the signal and the frequency as well as the capacitance of the transient suppressor should be considered. The current through CP is a function of dv/dt and the distortion is a function of the signal's source impedance.

Each case must be evaluated individually to determine the maximum allowable capacitance. The structural characteristics of metal-oxide varistors unavoidably result in an appreciable capacitance between the device terminals, depending on area, thickness and material processing. For the majority of power applications, this capacitance can be of benefit. In high-frequency applications, however, the effect must be taken into consideration in the overall system design.

3.5.1.12 References

For Littelfuse documents available on the web, see http://www.littelfuse.com/

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3.6 Littelfuse Varistors.

3.6.1 Basic Properties, Terminology and Theory

***Application Note July 1999*AN9767.1**

3.6.2 What Is A Littelfuse Varistor?

Varistors are voltage dependent, nonlinear devices which have an electrical behavior similar to back-to-back zener diodes. The symmetrical, sharp breakdown characteristics shown in Figure 1 enable the varistor to provide excellent transient suppression performance. When exposed to high voltage transients the varistor impedance changes many orders of magnitude from a near open circuit to a highly conductive level, thus clamping the transient voltage to a safe level. The potentially destructive energy of the incoming transient pulse is absorbed by the varistor, thereby protecting vulnerable circuit components.

The varistor is composed primarily of zinc oxide with small additions of bismuth, cobalt, manganese and other metal oxides. The structure of the body consists of a matrix of conductive zinc oxide grains separated by grain boundaries providing P-N junction semiconductor characteristics. These boundaries are responsible for blocking conduction at low voltages and are the source of the nonlinear electrical conduction at higher voltages.

Since electrical conduction occurs, in effect, between zinc oxide grains distributed throughout the bulk of the device, the Littelfuse Varistor is inherently more rugged than its single PN junction counterparts, such as zener diodes. In the varistor, energy is absorbed uniformly throughout the body of the device with the resultant heating spread evenly through its volume. Electrical properties are controlled mainly by the physical dimensions of the varistor body which is sintered in various form factors such as discs, chips and tubes. The energy rating is determined by volume, voltage rating by thickness or current flow path length, and current capability by area measured normal to the direction of current flow.

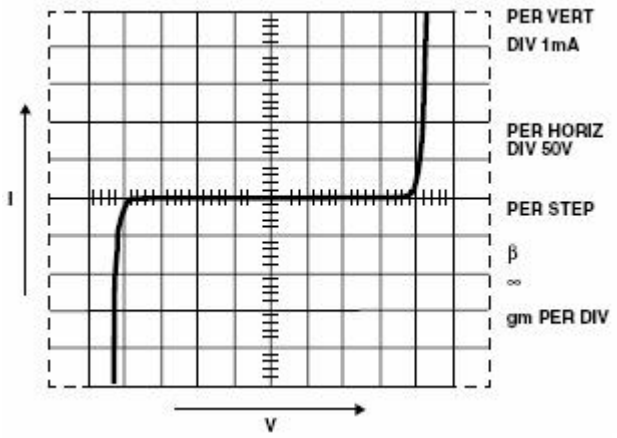


FIGURE 1. TYPICAL VARISTOR V-I CHARACTERISTIC

Littelfuse Varistors are available with AC operating voltages from 2.5V to 6000V. Higher voltages are limited only by packaging ability. Peak current handling exceeds 70,000A and energy capability extends beyond 10,000J for the larger units. Package styles include the tiny multilayer surface mount suppressors, tubular devices for use in connectors, and progress in size up to the rugged industrial device line.

3.6.3 Physical Properties Introduction

An attractive property of the metal oxide varistor, fabricated from zinc oxide (ZnO), is that the electrical characteristics are related to the bulk of the device. Each ZnO grain of the ceramic acts as if it has a semiconductor junction at the grain boundary. A cross-section of the material is shown in Figure 2, which illustrates the ceramic microstructure. The ZnO grain boundaries can be clearly observed. Since the nonlinear electrical behavior occurs at the boundary of each semiconducting ZnO grain, the varistor can be considered a "multi-junction" device composed of many series and parallel connections of grain boundaries. Device behavior may be analyzed with respect to the details of the ceramic microstructure. Mean grain size and grain size distribution play a major role in electrical behavior.

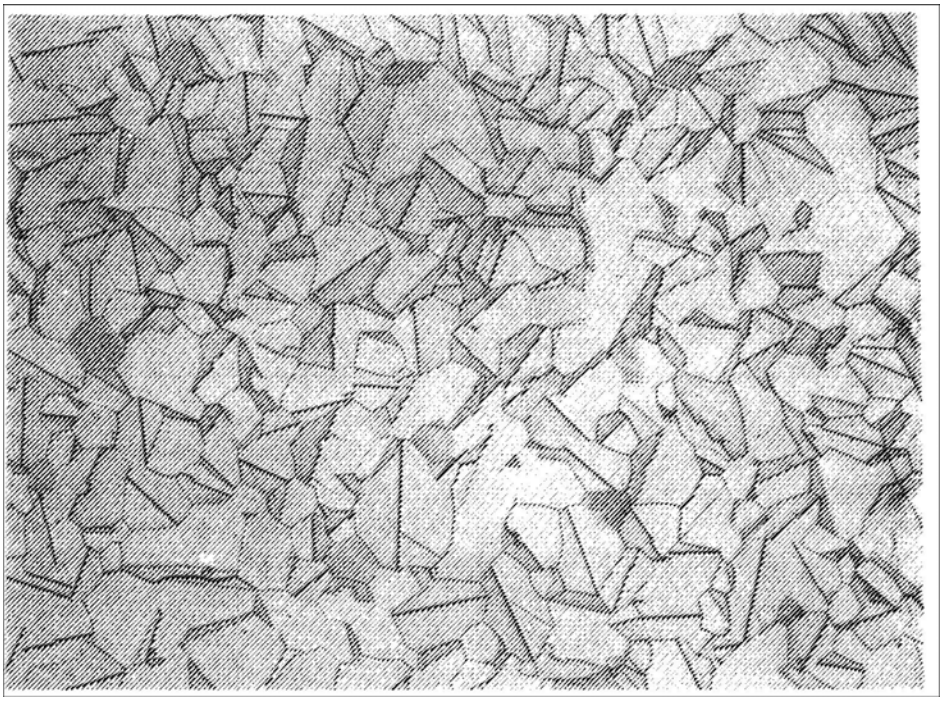


FIGURE 2. OPTICAL PHOTOMICROGRAPH OF A POLISHED AND ETCHED SECTION OF A VARISTOR

3.6.4 Varistor Microstructure

Varistors are fabricated by forming and sintering zinc oxide-based powders into ceramic parts. These parts are then electroded with either thick film silver or arc/flame sprayed metal. The bulk of the varistor between contacts is comprised of ZnO grains of an average size "d" as shown in the schematic model of Figure 3. Resistivity of the ZnO is <0.3 Ω -cm.

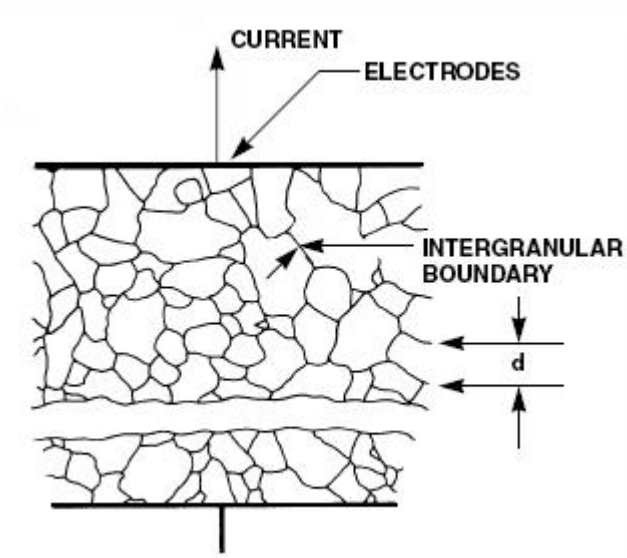


FIGURE 3. SCHEMATIC DEPICTION OF THE MICROSTRUCTURE OF A METAL-OXIDE VARISTOR. GRAINS OF CONDUCTING ZnO (AVERAGE SIZE d) ARE SEPARATED BY INTERGRANULAR BOUNDARIES

Designing a varistor for a given nominal varistor voltage, V N, is basically a matter of selecting the device thickness such that the appropriate number of grains, n, are in series between electrodes. In practice, the varistor material is characterized by a voltage gradient measured across its thickness by a specific volts/mm value. By controlling composition and manufacturing conditions the gradient remains fixed. Because there are practical limits to the range of thicknesses achievable, more than one voltage gradient value is desired. By altering the composition of the metal oxide additives it is possible to change the grain size "d" and achieve the desired result.

A fundamental property of the ZnO varistor is that the voltage drop across a single interface "junction" between grains is nearly constant. Observations over a range of compositional variations and processing conditions show a fixed voltage drop of about 2V-3V per grain boundary junction. Also, the voltage drop does not vary for grains of different sizes. It follows, then, that the varistor voltage will be determined by the thickness of the material and the size of the ZnO grains.

The relationship can be stated very simply as follows:

Varistor Voltage, VN (DC) = (3V)n

Where, n = average number of grain boundaries between electrodes

and, varistor thickness, D = (n + 1)d

≈

(VN X d)/3

where, d = average grain size

The varistor voltage, VN , is defined as the voltage across a varistor at the point on its V-I characteristic where the transition is complete from the low-level linear region to the highly nonlinear region. For standard measurement purposes, it is arbitrarily defined as the voltage at a current of 1mA.

Some typical values of dimensions for Littelfuse Varistors are given in Table 1.

TABLE 1.

VARISTOR VOLTAGE	AVERAGE GRAIN SIZE		GRADIENT	DEVICE THICKNESS
VOLTS	MICRONS	n	V/mm AT 1mA	mm
$150V_{RMS}$	20	75	150	1.5
$25V_{RMS}$	80 (Note)	12	39	1.0

NOTE: Low voltage formulation.

3.6.5 Theory of Operation

Because of the polycrystalline nature of metal-oxide semiconductor varistors, the physical operation of the device is more complex than that of conventional semiconductors.

Intensive measurement has determined many of the device's electrical characteristics, and much effort continues to better define the varistor's operation. In this application note we will discuss some theories of operation, but from the user's viewpoint this is not nearly as important as understanding the basic electrical properties as they relate to device construction.
The key to explaining metal-oxide varistor operation lies in understanding the electronic phenomena occurring near the grain boundaries, or junctions between the zinc oxide grains.

While some of the early theory supposed that electronic tunneling occurred through an insulating second phase layer at the grain boundaries, varistor operation is probably better described by a series-parallel arrangement of semiconducting diodes. In this model, the grain boundaries contain defect states which trap free electrons from the n-type semiconducting

zinc oxide grains, thus forming a space charge depletion layer in the ZnO grains in the region adjacent to the grain boundaries [6].

Evidence for depletion layers in the varistor is shown in Figure 4 where the inverse of the capacitance per boundary squared is plotted against the applied voltage per boundary [7]. This is the same type of behavior observed for semiconductor abrupt P-N junction diodes. The relationship is:

$$1/C2 = [2(Vb + V)]/(q\varepsilon sN)$$

Where Vb is the barrier voltage, V the applied voltage, q the electron charge, ε s the semiconductor permittivity and N is the carrier concentration. From this relationship the ZnO carrier concentration, N, was determined to be about 2 x 10 17 per cm 3 [7]. In addition, the width of the depletion layer was calculated to be about 1000 Angstrom units.

Single junction studies also support the diode model [9].
It is these depletion layers that block the free flow of carriers and are responsible for the low voltage insulating behavior in the leakage region as depicted in Figure 5. The leakage current is due to the free flow of carriers across the field lowered barrier, and is thermally activated, at least above about 25 o C.

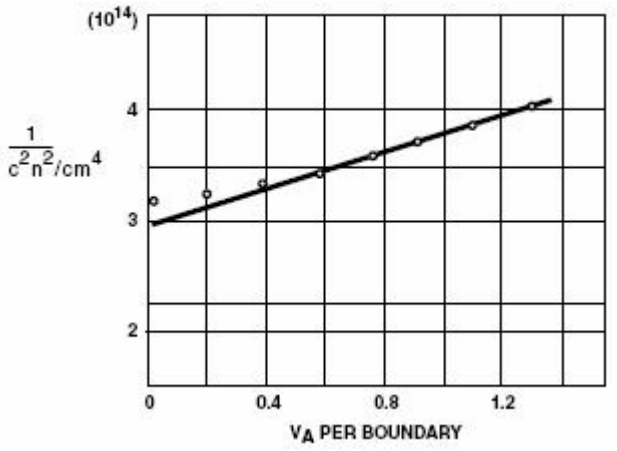


FIGURE 4. CAPACITANCE-VOLTAGE BEHAVIOR OF VARISTOR RESEMBLES A SEMICONDUCTOR ABRUPT-JUNCTION REVERSED BIASED DIODE Nd ~ 2 x 1017/cm3

Figure 5 shows an energy band diagram for a ZnO-grain boundary-ZnO junction [10].

The left-hand grain is forward biased, VL, and the right side is reverse biased to VR. The depletion layer widths are XL and XR, and the respective barrier heights are φL and φR.

The zero biased barrier height is φO . As the voltage bias is increased, φL is decreased and φR is increased, leading to a lowering of the barrier and an increase in conduction.
The barrier height φL of a low voltage varistor was measured as a function of applied voltage [11], and is presented in Figure 6. The rapid decrease in the barrier at high voltage represents the onset of nonlinear conduction [12].

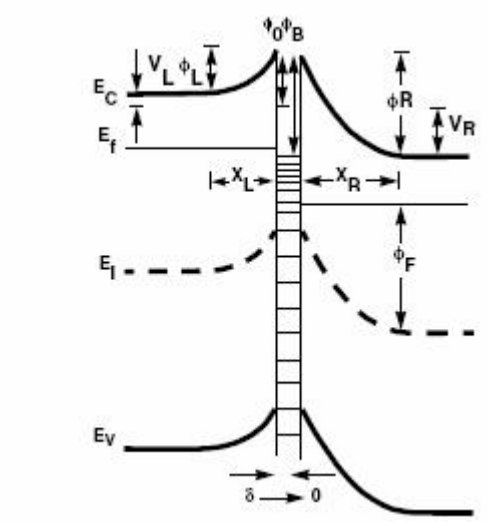


FIGURE 5. ENERGY BAND DIAGRAM OF A ZnO-GRAINBOUNDARY-ZnO JUNCTION

Transport mechanisms in the nonlinear region are very complicated and are still the subject of active research. Most theories draw their inspiration from semiconductor transport theory and the reader is referred to the literature for more information [3, 5, 13, 14, 15].

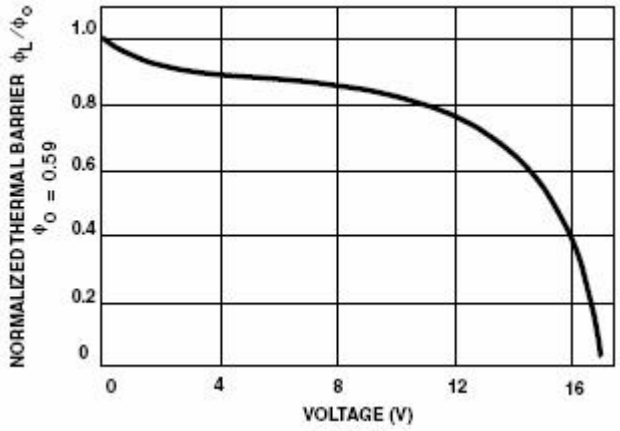


FIGURE 6. THERMAL BARRIER vs APPLIED VOLTAGE

Turning now to the high current upturn region in Figure 10, we see that the V-I behavior approaches an ohmic characteristic. The limiting resistance value depends upon the electrical conductivity of the body of the semiconducting ZnO grains, which have carrier concentrations in the range of 10 17 to 10 18 per cm 3 . This would put the ZnO resistivity below 0.3 Ω cm.

3.6.6 Varistor Construction

The process of fabricating a Littelfuse Varistor is illustrated in the flow chart of Figure 7. The starting material may differ in the composition of the additive oxides, in order to cover the voltage range of product.

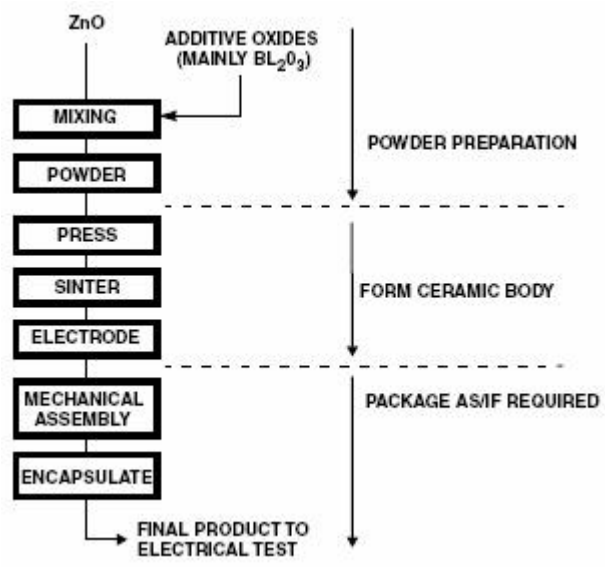


FIGURE 7. SCHEMATIC FLOW DIAGRAM OF LITTELFUSE VARISTOR FABRICATION

Device characteristics are determined at the pressing operation. The powder is pressed into a form of predetermined thickness in order to obtain a desired value of nominal voltage. To obtain the desired ratings of peak current and energy capability, the electrode area and mass of the device are varied. The range of diameters obtainable in disc product offerings is listed here:

Nominal Disc Diameter mm	3	5	7	10	14	20	32	34	40	62

Of course, other shapes, such as rectangles, are also possible by simply changing the press dies. Other ceramic fabrication techniques can be used to make different shapes.

For example, rods or tubes are made by extruding and cutting to length. After forming, the green (i.e., unfired) parts are placed in a kiln and sintered at peak temperatures in excess of 1200 oC. The bismuth oxide is molten above 825 oC, assisting in the initial densification of

the polycrystalline ceramic. At higher temperatures, grain growth occurs, forming a structure with controlled grain size.

Electroding is accomplished, for radial and chip devices, by means of thick film silver fired onto the ceramic surface. Wire leads or strap terminals are then soldered in place. A conductive epoxy is used for connecting leads to the axial 3mm discs. For the larger industrial devices (40mm and 60mm diameter discs) the contact material is arc sprayed aluminum, with an overspray of copper if necessary to give a solderable surface.

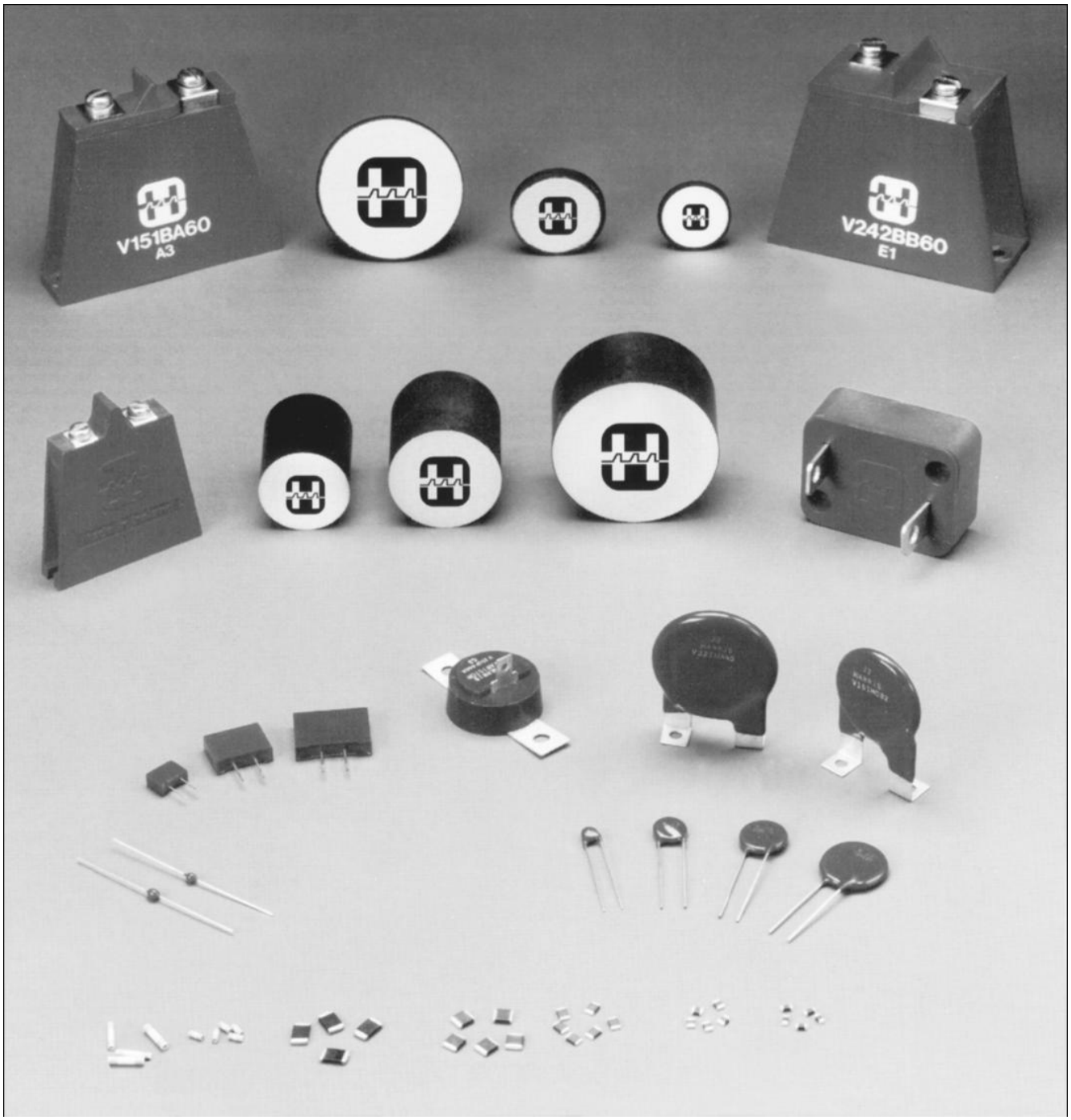
Many encapsulation techniques are used in the assembly of the various Littelfuse Varistor packages. Most radials and some industrial devices (HA Series) are epoxy coated in a fluidized bed, whereas epoxy is "spun" onto the axial device.

Radials are also available with phenolic coatings applied using a wet process. The PA series package consists of plastic molded around a 20mm disc subassembly. The RA, DA, and DB series devices are all similar in that they all are composed of discs or chips, with tabs or leads, encased in a molded plastic shell filled with epoxy. Different package styles allow variation in energy ratings, as well as in mechanical mounting. Figures 8 and 9 illustrate several package forms. Figure 9 shows construction details of some packages. Dimensions of the ceramic, by package type, are given in Table 2.

TABLE 2. BY-TYPE CERAMIC DIMENSIONS

PACKAGE TYPE	SERIES	CERAMIC DIMENSIONS
Leadless Surface Mount	CH, AUML†, ML†, MLE† MLN† Series	5mm x 8mm Chip, 0603, 0805, 1206, 1210, 1812, 2220
Connector Pin	CP Series	22, 20, 16 ID Gauge Tube
Axial Leaded	MA Series	3mm Diameter Disc
Radial Leaded	ZA, LA, "C" III, UltraMOV™ Series	5mm, 7mm, 10mm, 14mm, 20mm Diameter Discs
Boxed, Low Profile	RA Series	5mm x 8mm, 10mm x 16mm, 14 x 22 Chips
Industrial Packages	PA Series HA Series HB Series DA, DB Series BA, BB Series	20mm Diameter Disc 32mm, 40mm Diameter Disc 34mm Square Disc 40mm Diameter Disc 60mm Diameter Disc
Industrial Discs	CA, NA Series	32mm, 40mm, 60mm Diameter Discs, 34mm Square
Arrester	AS Series	32mm, 42mm, 60mm Diameter Discs

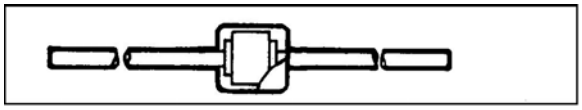
†Littelfuse multilayer suppressor technology devices.


V151BA60
A3
V242BB60
E1

3.6.7 Electrical Characterization

3.6.7.1 Varistor VI Characteristics

FIGURE 9A. CROSS-SECTION OF MAPACKAGE



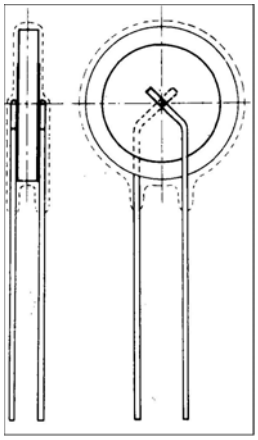
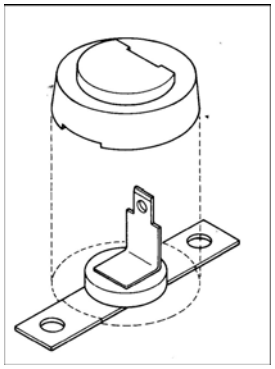
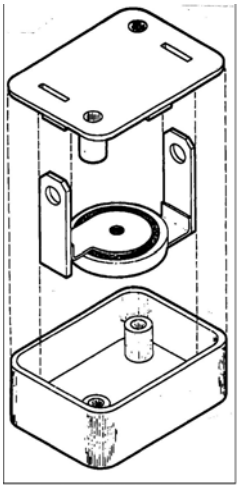


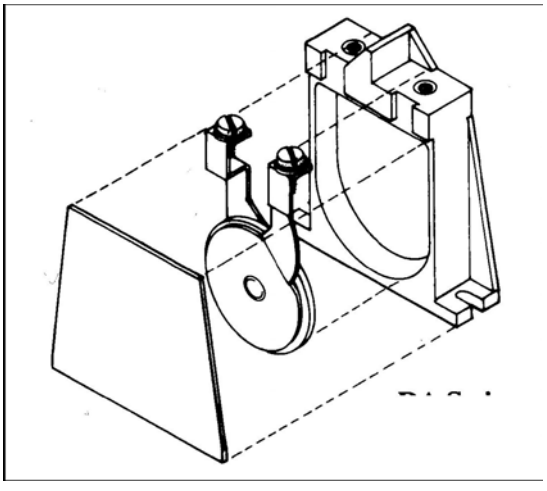
FIGURE 9B. CROSS-SECTION OF RADIAL LEAD PACKAGE



PA SERIES
FIGURE 9C. PICTORIAL VIEW OF POWER MOV PACKAGE

DB SERIES **DA SERIES** **BA/BB SERIES**





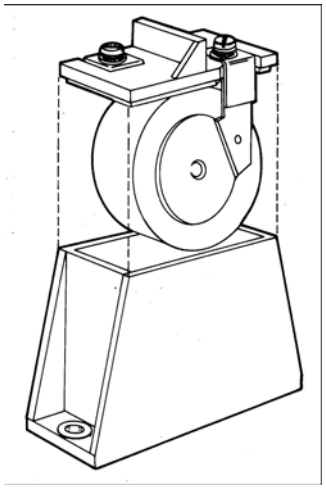


FIGURE 9D. PICTORIAL VIEW OF HIGH ENERGY PACKAGES, DA, DB, AND BA/BB SERIES

Varistor electrical characteristics are conveniently displayed using log-log format in order to show the wide range of the V-I curve. The log format also is clearer than a linear representation which tends to exaggerate the nonlinearity in proportion to the current scale chosen. A typical V-I characteristic curve is shown in Figure 10. This plot shows a wider range of current than is normally provided on varistor data sheets in order to illustrate three distinct regions of electrical operation.

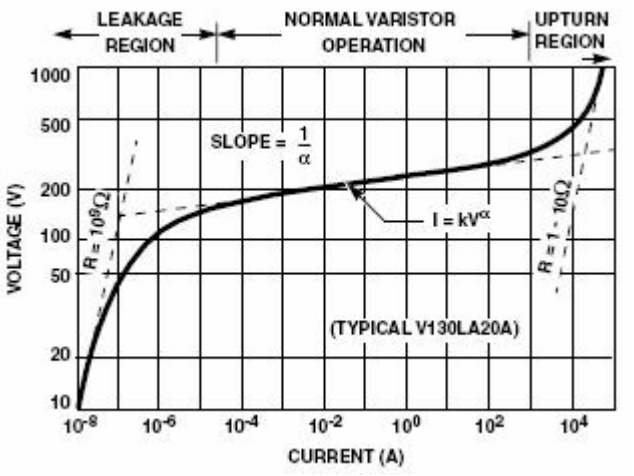


FIGURE 10. TYPICAL VARISTOR V-I CURVE PLOTTED ON LOG-LOG SCALE

3.6.7.2 Equivalent Circuit Model

An electrical model for the varistor can be represented by the simplified equivalent circuit of Figure 11.

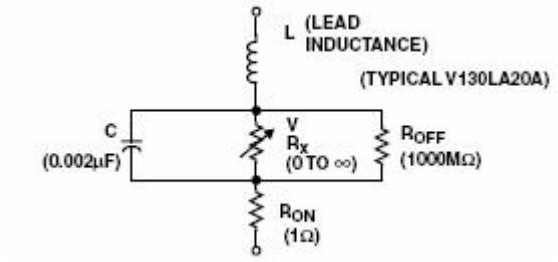


FIGURE 11. VARISTOR EQUIVALENT CIRCUIT MODEL

3.6.7.3 Leakage Region of Operation

At low current levels, the V-I Curve approaches a linear (ohmic) relationship and shows a significant temperatura dependence. The varistor is in a high resistance mode (approaching 109 Ω) and appears as an open circuit. The nonlinear resistance component, RX, can be ignored because ROFF in parallel will predominate. Also, RON will be insignificant compared to ROFF.

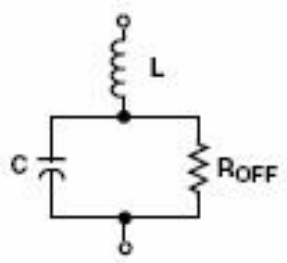


FIGURE 12. EQUIVALENT CIRCUIT AT LOW CURRENTS

For a given varistor device, capacitance remains approximately constant over a wide range of voltage and frequency in the leakage region. The value of capacitance drops only slightly as voltage is applied to the varistor. As the voltage approaches the nominal varistor voltage, the capacitance abruptly decreases. Capacitance remains nearly constant with frequency change up to 100kHz. Similarly, the change with temperature is small, the 25 oC value of capacitance being well within ☐} 10% from –40 oC to 125 oC.

The temperature effect of the V-I characteristic curve in the leakage region is shown in Figure 13. A distinct temperature dependence is noted.

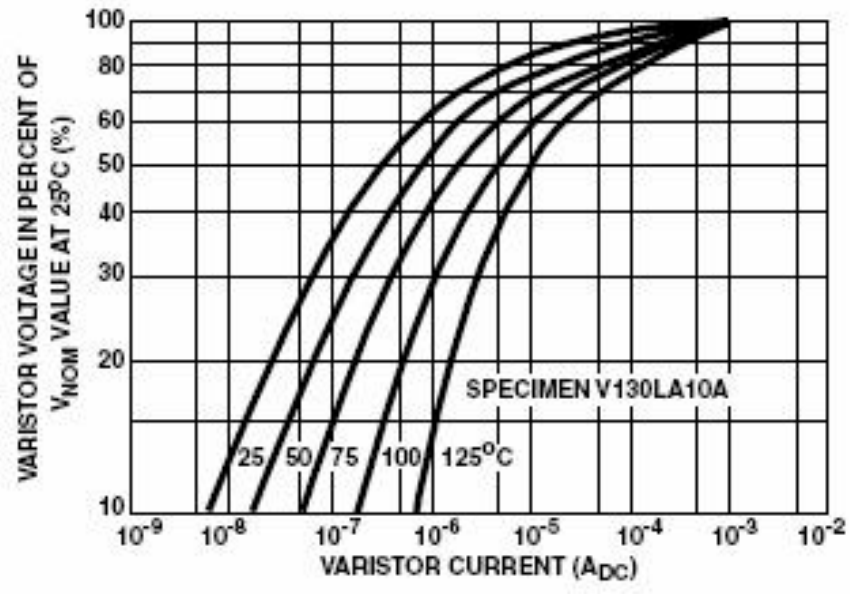


FIGURE 13. TEMPERATURE DEPENDENCE OF THE CHARACTERISTIC CURVE IN THE LEAKAGE REGION

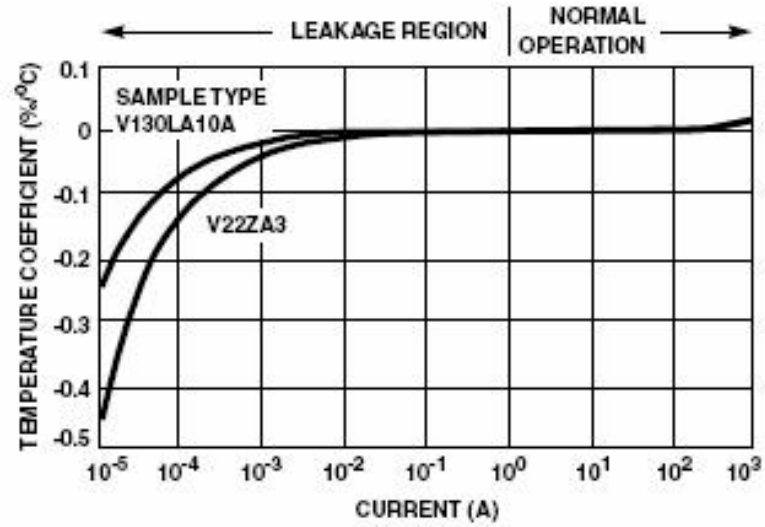
The relation between the leakage current, I, and temperature, T, is:

$I = IO\ \varepsilon^{-VB/kT}$

where: IO = constant
k = Boltzmann's Constant
VB = 0.9eV

The temperature variation, in effect, corresponds to a change in ROFF. However, ROFF remains at a high resistance value even at elevated temperatures. For example, it is still in the range of 10M Ω to 100MΩ at 125 oC.

Although ROFF is a high resistance it varies with frequency. The relationship is approximately linear with inverse frequency.
ROFF ~ 1/f
However, the parallel combination of ROFF and C is predominantly capacitive at any frequency of interest. This is because the capacitive reactance also varies approximately linearly with 1/f.
At higher currents, at and above the milliamp range, temperature variation becomes minimal. The plot of the temperature coefficient (DV/DT) is given in Figure 14. It should be noted that the temperature coefficient is negative and decreases as current rises. In the clamping voltage range of the varistor (I > 1A), the temperature dependency approaches zero.



NOTE: Typical Temperature Coefficient of Voltage vs Current, 14mm Size, 55°C to 125°C.

FIGURE 14. RELATION OF TEMPERATURE COEFFICIENT DV/DT TO VARISTOR CURRENT

3.6.7.4 Normal Varistor Region of Operation

The varistor characteristic follows the equation I = kVα, where k is a constant and the exponent α defines the degree of nonlinearity. Alpha is a figure of merit and can be determined from the slope of the V-I curve or calculated from the formula:

$$\alpha = [\log(I2 / I1)]/[\log(V2 / V1)]$$

$$1/\log(V2 / V1) \text{ for } I2 / I1 = 1$$

In this region the varistor is conducting and RX will predominate over C, RON and ROFF. RX becomes many orders of magnitude less than ROFF but remains larger than RON.

FIGURE 15. EQUIVALENT CIRCUIT AT VARISTOR CONDUCTION

During conduction the varistor voltage remains relatively constant for a change in current of several orders of magnitude. In effect, the device resistance, RX, is changing in response to current. This can be observed by examining the static or dynamic resistance as a function of current. The static resistance is defined by:

$$R_X = V/I$$

and the dynamic resistance by:

$$Z_X = dv/di = V / \alpha I = R_X / \alpha$$

Plots of typical resistance values vs current, I, are given in Figure 16.

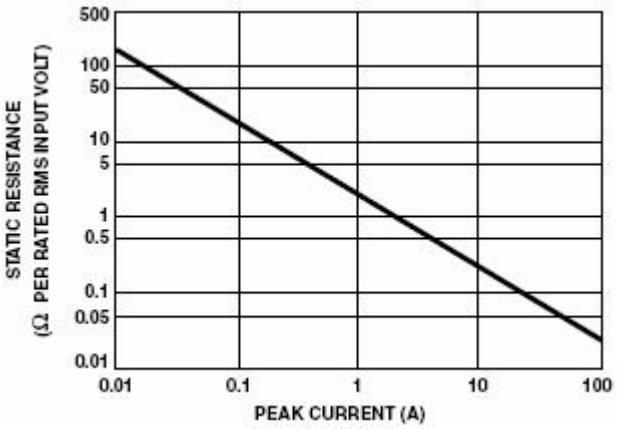


FIGURE 16A. RX STATIC VARISTOR RESISTANCE FIGURE

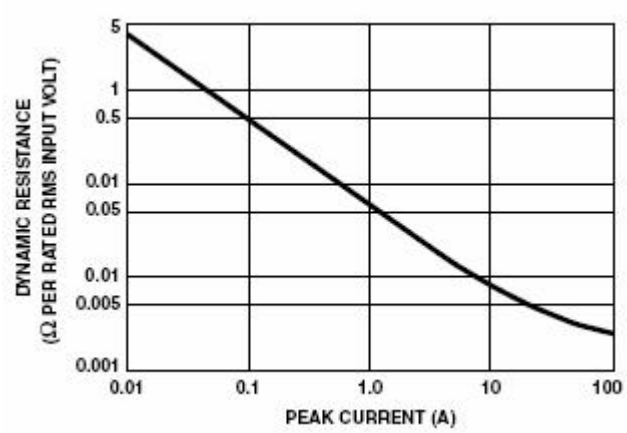


FIGURE 16B. ZX DYNAMIC VARISTOR RESISTANCE

3.6.8 Upturn Region of Operation

At high currents, approaching the maximum rating, the varistor approximates a short-circuit. The curve departs from the nonlinear relation and approaches the value of the material bula resistance, about 1Ω-10Ω. The upturn takes place as RX approaches the value of RON. Resistor RON represents the bulk resistance of the zinc oxide grains. This resistance is linear (which appears as a steeper slope on the log plot) and occurs at currents 50A to 50,000A, depending on the varistor size.

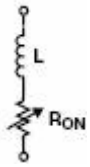


FIGURE 17. EQUIVALENT CIRCUIT AT VARISTOR UPTURN

3.6.9 Speed of Response and Rate Effects

The varistor action depends on a conduction mechanism similar to that of other semiconductor devices. For this reason, conduction occurs very rapidly, with no apparent time lag - even into the nanosecond range. Figure 18 shows a composite photograph of two voltage traces with and without a varistor inserted in a very low inductance impulse generator. The second trace (which is not synchronized with the first, but merely superimposed on the oscilloscope screen) shows that the voltage clamping effect of the varistor occurs in less than one nanosecond.

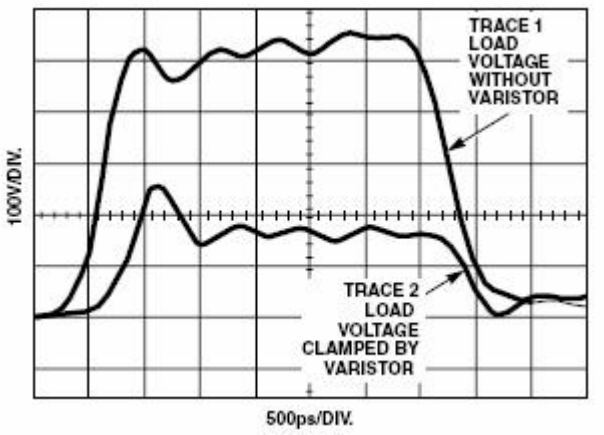


FIGURE 18. RESPONSE OF A ZnO VARISTOR TO A FAST RISE TIME (500ps) PULSE

In the conventional lead-mounted devices, the inductance of the leads would completely mask the fast action of the varistor; therefore, the test circuit for Figure 18 required insertion of a small piece of varistor material in a coaxial line to demonstrate the intrinsic varistor response. Tests made on lead mounted devices, even with careful attention to minimizing lead length, show that the voltages induced in the loop formed by the leads contribute a substantial part of the voltage appearing across the terminals of a varistor at high current and fast current rise.

Fortunately, the currents which can be delivered by a transient source are invariably slower in rise time than the observed voltage transients. The applications most frequently encountered for varistors involve current rise times longer than 0.5μs. Voltage rate-of-rise is not the best term to use when discussing the response of a varistor to a fast impulse (unlike spark gaps where a finite time is involved in switching from nonconducting to conducting state). The response time of the varistor to the transient current that a circuit can deliver is the appropriate characteristic to consider. The V-I characteristic of Figure 19A shows how the response of the varistor is affected by the current waveform. From such data, an "overshoot" effect can be defined as being the relative increase in the maximum voltage appearing across the varistor during a fast current rise, using the conventional 8/20μs current wave as the reference. Figure 19B shows typical clamping voltage variation with rise time for various current levels.

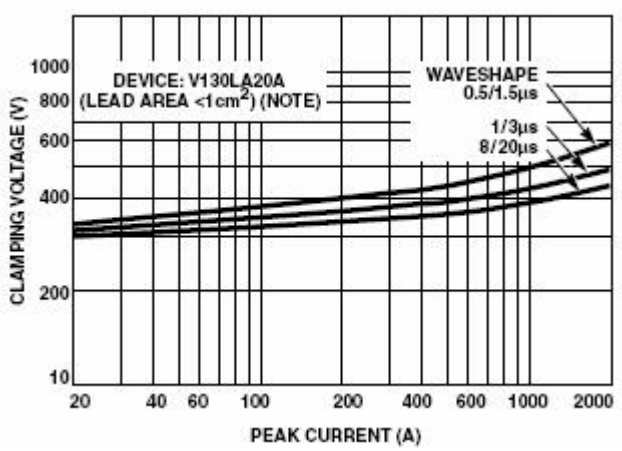


FIGURE 19A. V-I CHARACTERISTICS FOR VARIOUS CURRENT RISE TIMES

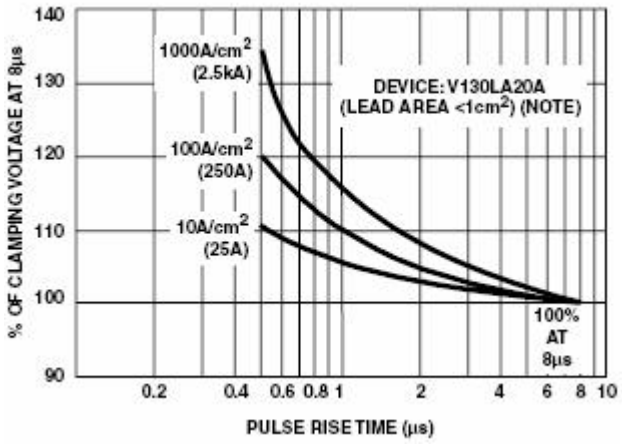


FIGURE 19B. OVERSHOOT DEFINED WITH REFERENCE TO THE BASIC 8/20µs CURRENT PULSE

NOTE: Refer to the Maximum Clamping Voltage section of DB450, Transient Voltage Suppression Devices.

FIGURE 19. RESPONSE OF LEAD-MOUNTED VARISTORS TO CURRENT WAVEFORM

3.6.10 Varistor Terminology

The following tabulation defines the terminology used in varistor specifications. Existing standards have been followed wherever possible.

3.6.11 Definitions (IEEE Standard C62.33, 1982)

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, or thermal, and can be expressed as a value for stated conditions.
A rating is a value which establishes either a limiting capability or a limiting condition (either maximum or minimum) for operation of a device. It is determined for specified values of environment and operation. The ratings indicate a level of stress which may be applied to the device without causing degradation or failure. Varistor symbols are defined on the linear V-I graph illustrated in Figure 20.

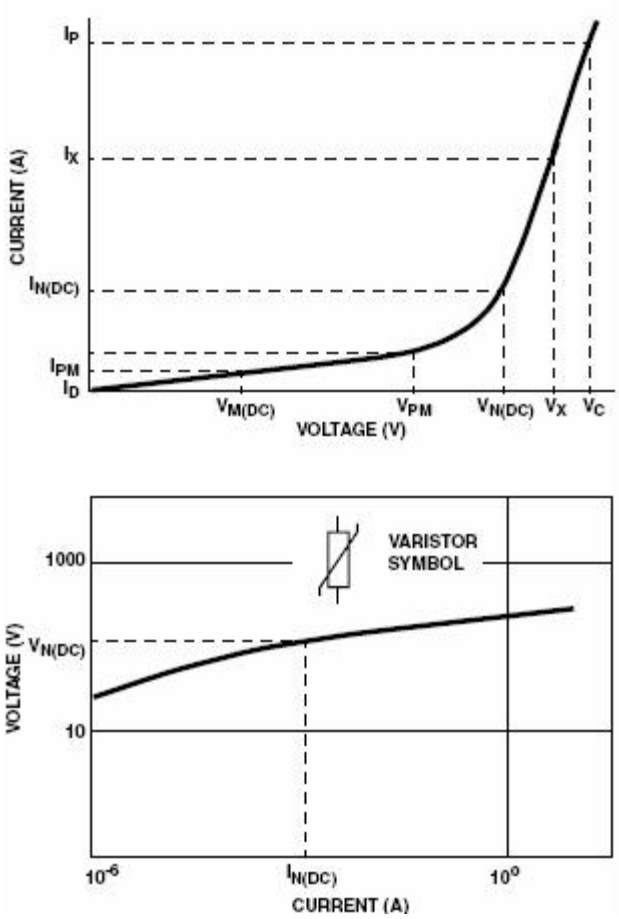


FIGURE 20. I-V GRAPH ILLUSTRATING SYMBOLS AND DEFINITIONS

3.6.12 Test Waveform

At high current and energy levels, varistor characteristics are measured, of necessity, with an impulse waveform. Shown in Figure 21 is the ANSI Standard C62.1 waveshape, an exponentially decaying waveform representative of lightning surges and the discharge of stored energy in reactive circuits.

The 8/20μs current wave (8μs rise and 20μs to 50% decay of peak value) is used as a standard, based on industry practices, for the characteristics and ratings described. One exception is the energy rating (WTM), where a longer waveform of 10/1000μs is used. This condition is more representative of the high energy surges usually experienced from inductive discharge of motors and transformers. Varistors are rated for a maximum pulse energy surge that results in a varistor voltage (VN) shift of less than ☐}10% from initial value.

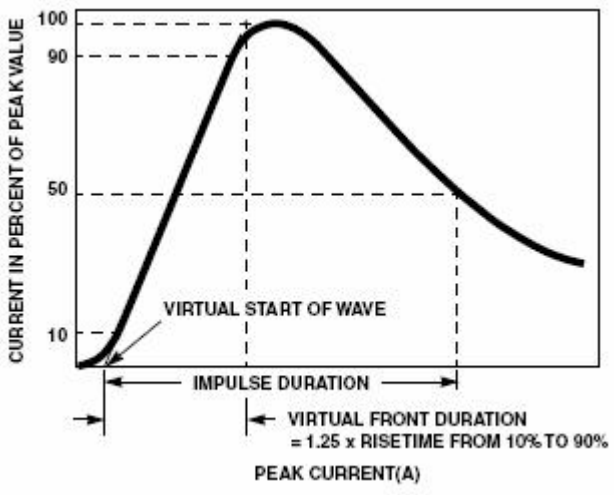


FIGURE 21. DEFINITION OF PULSE CURRENT WAVEFORM

TABLE 3. VARISTOR CHARACTERISTICS (IEEE STANDARD C62.33-1982 SUBSECTION 2.3 AND 2.4

TERMS AND DESCRIPTIONS	SYMBOL
Clamping Voltage. Peak voltage across the varistor measured under conditions of a specified peak VC pulse current and specified waveform. NOTE: Peak voltage and peak currents are not necessarily coincidental in time.	VC
Rated Peak Single Pulse Transient Currents (Varistor). Maximum peak current which may be applied for a single 8/20μs impulse, with rated line voltage also applied, without causing device failure.	ITM
Lifetime Rated Pulse Currents (Varistor). Derated values of ITM for impulse durations exceeding that of an 8/20μs waveshape, and for multiple pulses which may be applied over device rated lifetime.	-
Rated RMS Voltage (Varistor). Maximum continuous sinusoidal RMS voltage which may be applied.	VM(AC)
Rated DC Voltage (Varistor). Maximum continuous DC voltage which may be applied.	VM(DC)
DC Standby Current (Varistor). Varistor current measured at rated voltage, VM(DC).	ID
For certain applications, some of the following terms may be useful.	
Nominal Varistor Voltage. Voltage across the varistor measured at a specified pulsed DC current, IN(DC), of specific duration. IN(DC) of specific duration. IN(DC) is specified by the varistor manufacturer.	VN(DC)
Peak Nominal Varistor Voltage. Voltage across the varistor measured at a specified peak AC current, IN(AC), of specific duration. IN(AC) is specified by the varistor manufacturer.	VN(AC)
Rated Recurrent Peak Voltage (Varistor). Maximum recurrent peak voltage which may be applied for a specified duty cycle and waveform.	VPM
Rated Single Pulse Transient Energy (Varistor). Energy which may be dissipated for a single impulse of maximum rated current at a specified waveshape, with rated RMS voltage or rated DC voltage also applied, without causing device failure.	WTM
Rated Transient Average Power Dissipation (Varistor). Maximum average power which may be dissipated due to a group of pulses occurring within a specified isolated time period, without causing device failure.	PT(AV)M
Varistor Voltage. Voltage across the varistor measured at a given current, IX.	VX
Voltage Clamping Ratio (Varistor). A figure of merit measure of the varistor clamping effectiveness as defined by the symbols VC/VM(AC), VC/VM(DC).	VC/VPM

TERMS AND DESCRIPTIONS	SYMBOL
Nonlinear Exponent. A measure of varistor nonlinearity between two given operating currents, I1 and I2, as described by $I = kV\alpha$ where k is a device constant, $I1 \leq I \leq I2$, and $\alpha_{12} = \log (I_2 / I_1)/\log (V_2 / V_1)$	α
Dynamic Impedance (Varistor). A measure of small signal impedance at a given operating point as defined by: ZX = dVX/dIX	ZX
Resistance (Varistor). Static resistance of the varistor at a given operating point as defined by: RX = VX/IX	RX
Capacitance (Varistor). Capacitance between the two terminals of the varistor measured at C specified frequency and bias.	C
AC Standby Power (Varistor). Varistor AC power dissipation measured at rated RMS voltage VM(AC).	PD
Voltage Overshoot (Varistor). The excess voltage above the clamping voltage of the device for a given current that occurs when current waves of less than 8μs virtual front duration are applied. This value may be expressed as a % of the clamping voltage (VC) for an 8/20 current wave.	VOS
Response Time (Varistor). The time between the point at which the wave exceeds the clamping voltage level (VC) and the peak of the voltage overshoot. For the purpose of this definition, clamping voltage as defined with an 8/20μs current waveform of the same peak current amplitude as the waveform used for this response time.	-
Overshoot Duration (Varistor). The time between the point voltage level (VC) and the point at which the voltage overshoot has decayed to 50% of its peak. For the purpose of this definition, clamping voltage is defined with an 8/20μs current waveform of the same peak current amplitude as the waveform used for this overshoot duration.	-

3.7 How to Connect a Littelfuse Varistor

Transient suppressors can be exposed to high currents for short durations in the nanoseconds to millisecond time frame.
Littelfuse Varistors are connected in parallel to the load, and any voltage drop in the leads to the varistor will reduce its effectiveness. Best results are obtained by using short leads that are close together to reduce induced voltages and a low ohmic resistance to reduce I • R drops.

3.7.1 Electrical Connections

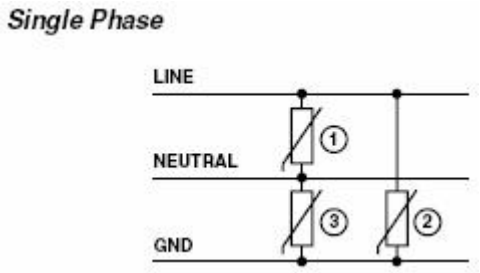
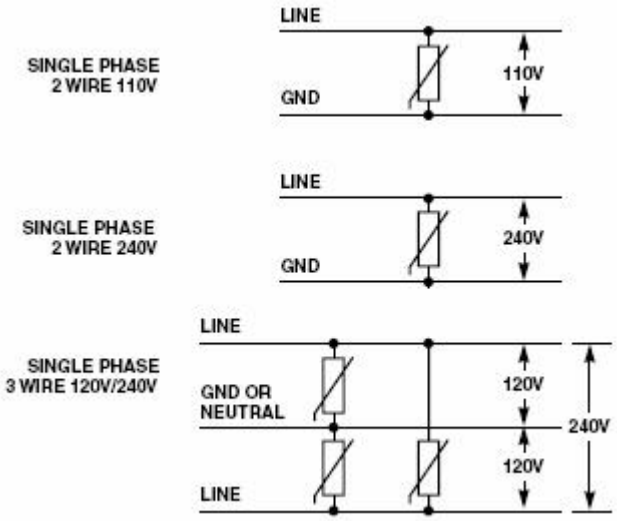


Figure 22

Figure 23



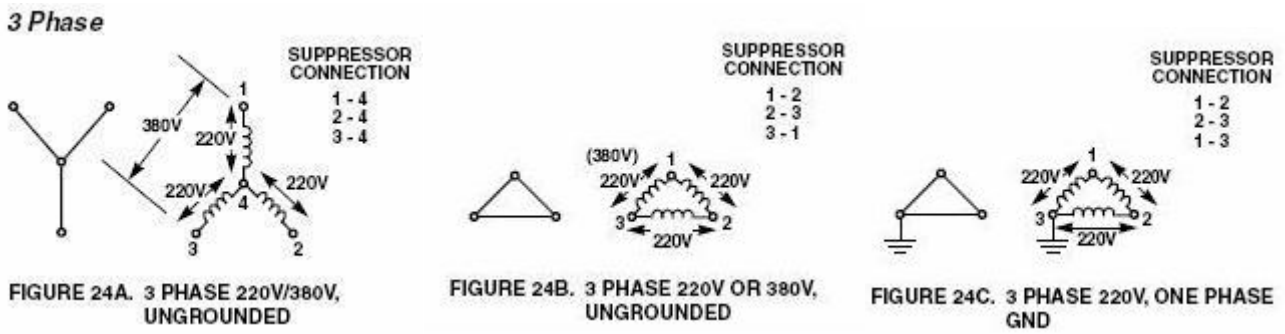


FIGURE 24A. 3 PHASE 220V/380V, UNGROUNDED

FIGURE 24B. 3 PHASE 220V OR 380V, UNGROUNDED

FIGURE 24C. 3 PHASE 220V, ONE PHASE GND

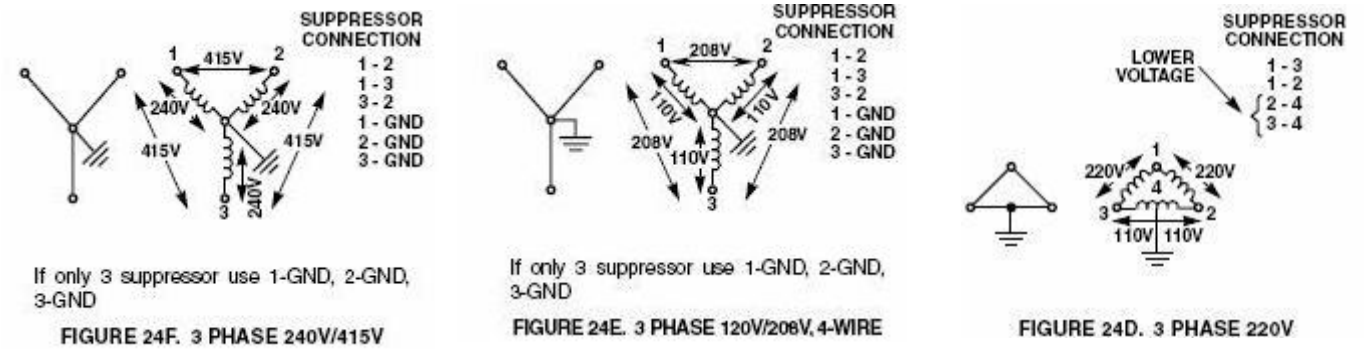


FIGURE 24F. 3 PHASE 240V/415V

FIGURE 24E. 3 PHASE 120V/208V, 4-WIRE

FIGURE 24D. 3 PHASE 220V

Figure 24.

For higher voltages use same connections, but select varistors for the appropriate voltage rating.

3.7.2 DC Applications

DC applications require connection between plus and minus or plus and ground and minus and ground. For example, if a transient towards ground exists on all 3 phases (common mode transients) only transient suppressors connected phase to ground would absorb energy. Transient suppressors connected phase to phase would not be effective.

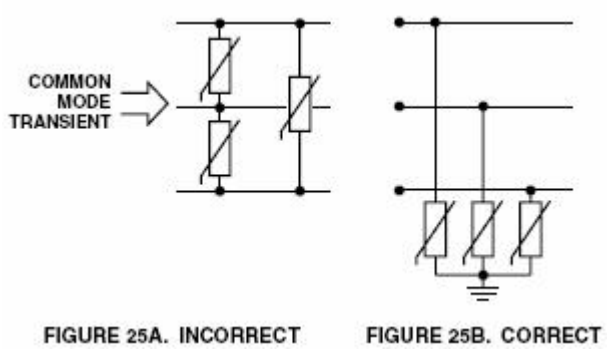


FIGURE 25. COMMON MODE TRANSIENT AND CORRECT SOLUTION

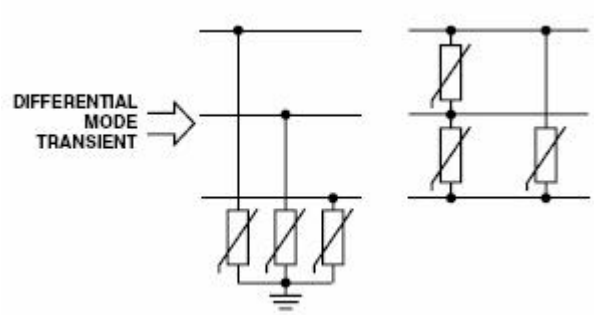


FIGURE 26. DIFFERENTIAL MODE TRANSIENT AND CORRECT SOLUTION

3.7.3 References

For Littelfuse documents available on the web, see http://www.littelfuse.com/

AUTOR	TITULO	EDITORIAL
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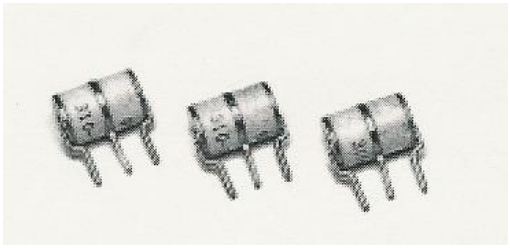
3.7.4 Application Note AN-111

3.7.4.1 AN 111: Surge Arrester Technologies

GAS DISCHARGE TUBE n AIR GAP n CARBON BLOCK n SCR n ZENER DIODE n MOV



In today's world of sensitive electronics, an increasingly important topic has become the protection of electronic components from over voltage surges. There is a multitude of devices on the market for this purpose but what are the differences between them and which is best for what application? The following describes, analyzes, and compares these devices in detail. Basically there are two types of surge protection classifications with each consisting of its own group of devices:

CROWBAR

- Air Gap
- Carbon Block
- Gas Discharge Tube (GDT)
- Silicon Controlled Rectifier (SCR)

CLAMP

- Zener (Avalanche) Diode
- Metal Oxide Varistor (MOV)

3.7.4.2 CROWBAR PROTECTION

A crowbar device limits the energy delivered to the protected circuit by abruptly changing from a high impedance state to a low impedance state in response to an elevated voltage level. Having been subjected to a sufficient voltage level the crowbar begins to conduct. While conducting, the voltage across the crowbar remains quite low (typically less than 15 volts for gas discharge tubes usually higher for the air gap and carbon block protectors) and thus, the majority of the transient's power is dissipated in the circuit's resistive elements and not in the protected circuit nor the crowbar itself. This allows the crowbar to be able to withstand and protect loads from higher voltage and/or higher current levels for a greater duration of time than clamping devices.

AIR GAP PROTECTOR

An air gap protector consists of two conductive surfaces with a spacing between them that will permit an arc when a specified potential is placed across the surfaces. The air gap is not a sealed device and therefore it must operate at atmospheric pressure and under the effects of the environment. Since the electrodes are exposed to the environment, they will often experience oxidation and corrosion which is not a problem common to an SRC gas discharge tube. These factors contribute to the air gap's high nominal breakdown voltage, wide breakdown voltage tolerance, and poor impulse response. Often an air gap is placed in parallel with a gas discharge tube or carbon block protector to provide back up protection in the event that the primary protection fails.

CARBON BLOCK PROTECTOR

A carbon block protector consists of a pair of carbon elements separated by a 0.003-0.004 inch air gap. When a specified potential is placed across the carbon surfaces an arc will be initiated. Like the air gap protector, the carbon block is an unsealed device and its performance suffers in the same manner as the air gap. Carbon block protectors are used mainly for telephone line protection but are being replaced, in most installations, with the more reliable and consistent gas discharge tubes.

GAS DISCHARGE TUBE (GDT)

SRC's GDT, a hermetically sealed gas filled ceramic tube with metal electrodes, is recognized for:

- Stable electrical parameters
- High insulation resistance
- Low capacitance
- High current capability
- Low leakage current
- Low arc voltages

For a gas tube to begin conduction, an electron within the sealed device must gain sufficient energy to initiate the ionization of the gas. Complete ionization of the gas takes place through electron collision. The events leading up to this phenomenon occur when a gas tube is subjected to a rising voltage potential. Once the gas is ionized, breakdown occurs and the gas tube changes from a high impedance state to a virtual short circuit and thus, any transient will be diverted from and will not reach the protected circuit. The arc voltage (the voltage across the gas tube while the gas tube is conducting) will typically be 15 volts. After the transient has passed, the GDT will extinguish and again appear as an open circuit. In order to insure gas tube turn off at the zero crossing in AC applications, the current through the GDT once the transient has passed, must be less than the follow-on current rating of the gas tube. The follow-on current requirement can easily be met by placing a resistor in series with the gas tube. SRC's AC series of gas discharge tube surge arresters were developed

specifically to protect AC power lines and normally will not require additional components to limit follow-on current. In DC applications, the gas discharge tube will extinguish as long as the device is operated within the specified holdover conditions. Holdover conditions involve the maximum bias voltage that can appear across a gas discharge tube under specified current conditions and still allow the gas discharge tube to turn off. Under normal operating conditions, the GDT shunted across a circuit, will act like an open switch with a high insulation resistance. The GDT's breakdown voltage is determined by electrode spacing, gas type (usually neon and/or argon), gas pressure (less than atmospheric), and the rate of rise of the transient. Breakdown voltage is defined as that voltage at which a crowbar type of surge arrester changes from a high impedance state to a low impedance state. The series is categorized by the breakdown voltage of each gas tube when a slowly rising transient is applied. For example: SRC's GDT, CG2230L gas tube, will breakdown at 230V (+/- 15%) when subjected to a ramp with a rate of rise of 500V/ second. The breakdown voltage response of a crowbar to transients with ramp rates of 1V/microsecond or less is referred to as the DC breakdown voltage level.

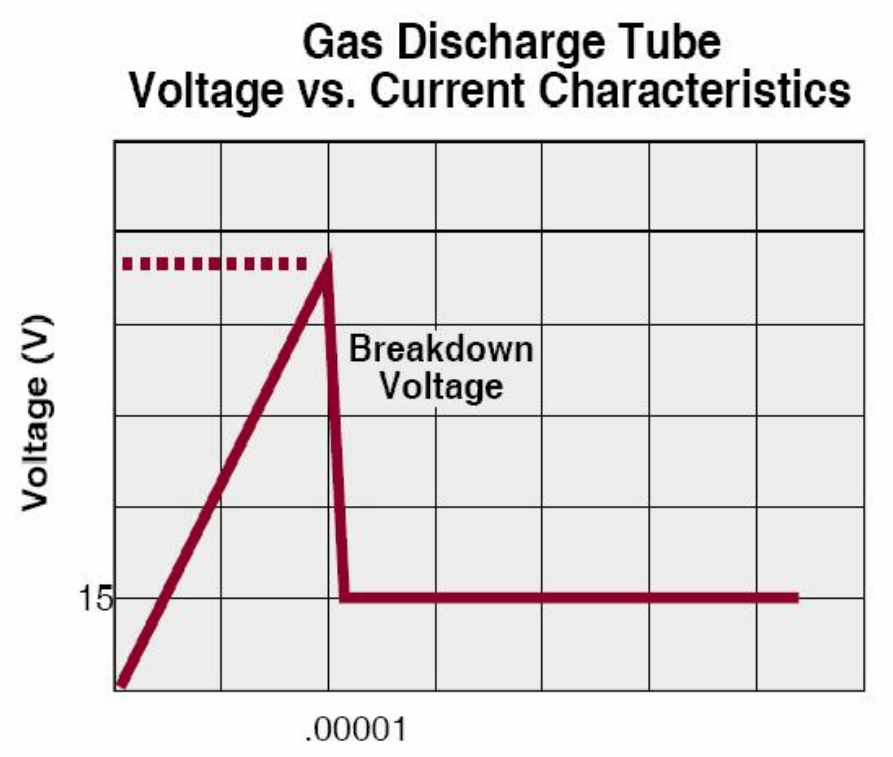


Figure 1

Due to the nature of gas discharge tubes, the same gas tube will experience breakdown at a higher voltage as a transient's ramp rate increases. For example: At 100V/microsecond, the CG2230L gas tube will breakdown at 600V maximum. The breakdown voltage response of a crowbar to transients with ramp rates greater than 1V/microsecond is referred to as the impulse breakdown voltage level. Due to the GDT's rugged construction, it can handle currents that far surpass other transient suppressors' capabilities - greater than 10 pulses of a 20,000 peak amperes pulse having a rise time of 8 microseconds decaying to half value in 20 microseconds (also referred to as an 8/20 wave form). The surge life of the GDT is at least 1000 shots of a 500 amperes peak 10/1000 pulse. Because it is being used in a repetitive

switching application, the ETS series GDT has been designed for surge life greater than 100,000 shots. With a maximum inter-electrode capacitance of 1 picofarad, the GDT can easily be designed into RF circuits. The GDT is the practical device for the protection of telephone circuits, AC power lines, modems, power supplies, CATV and almost any application where protection from large and/or unpredictable transients is desired.

SILICON CONTROLLED RECTIFIER (SCR)

Unlike the crowbar devices discussed above, the SCR is a semiconductor. Like the GDT, the SCR will have a very low voltage drop across it while conducting. The SCR does require a trigger signal when a surge is present before it can begin to conduct.
This trigger signal is usually supplied through the use of a zener diode. Packages that combine the SCR and zener diode are now available. These packages are monolithic devices and often contain an SCR-type thyristor with a gate region that acts like the avalanche diode. Once triggered, the SCR begins to conduct, dropping the voltage across the zener diode to a value below the zener's operating voltage and thus causing the zener to stop conducting. The SCR will conduct until the applied voltage drops to zero (zero crossing of AC) or until the current falls below a specified value (sometimes referred to as a holding current).
Although typically having a faster response time than a GDT, the SCR package is subject to higher leakage current and capacitance. The SCR package can handle currents of several hundred amperes of an 8/20 wave form and packages are available that offer bi-directional protection.

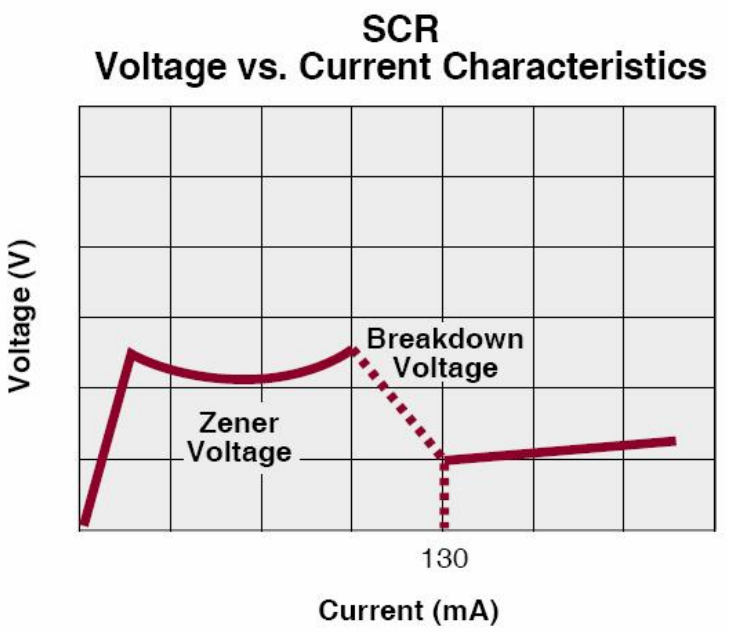


Figure 2

3.7.4.3 CLAMPING PROTECTION

A clamping device actually limits the voltage transient to a specified level by varying its internal resistance in response to the applied voltage. A clamping device must absorb the transient's energy and therefore, cannot withstand very high current levels. Although these

devices have quick response times, they are subject to leakage currents and their capacitance values are higher than those found in the GDT.

ZENER (AVALANCHE) DIODE

The zener diode comes closest to modeling the ideal constant voltage clamp. It responds quickly to a fast rising voltage potential and is available for a fairly wide range of clamping voltages (from less than 10 volts up to several hundred volts). The zener is placed in parallel with the circuit to be protected and will not operate until a surge exceeds the zener's breakdown voltage. The surge, causing the zener to conduct will be clamped to the zener's rated voltage. The zener is a good protector for circuits operating at low voltages. Caution is advised when designing the device into RF circuits due to the diode's high capacitance.

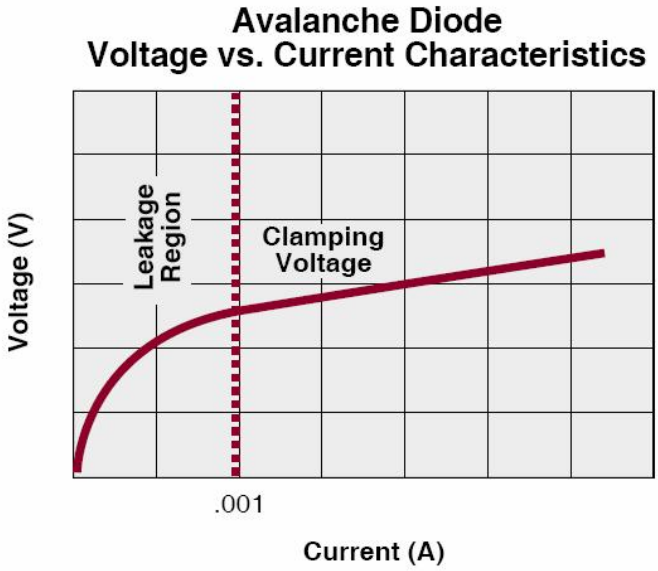


Figure 3

Also available are silcon avalanche suppressers which are referred to as transient voltage suppressers (TVS) diodes. These diodes consist of fairly large junction zeners which have been designed specifically for surge protection. The TVS diodes are rated for higher current surges than zener diodes and they can carry these currents for periods of 2-10 microseconds.
For use in AC signal lines, two zeners are required. These are available as packaged devices. Avalanche diodes are often used to protect IC's from static discharge and other forms of transients in power supplies computer buses, and data lines.

MOV (METAL OXIDE VARISTOR)

As its name suggests, the MOV is a voltage variable resistor made from sintered metal oxides. The grains produced in the sintered metal oxide material of the MOV can be thought of as a network of series and parallel diodes. As the voltage potential across the MOV increases, some of the diodes experience avalanche breakdown and begin to conduct and as a result, reduce the net resistance of the MOV.
The MOV can handle current pulses of higher peak values and for a longer duration than a diode, but the MOV can experience cumulative degradation and performance changes after it is exposed to large current pulses when not properly selected. The high peak current surges tend to fuse the oxide grains and thus alter the MOV's performance. Some engineers recommend that a fuse be used with an MOV as a large current surge could damage the grain structure, fuse the grains together and result in the protected circuit being shorted out. The MOV is available in a wide range of voltages and experiences a quick turn on time when subjected to a fast rising surge. The MOV is subject to leakage current and high capacitance (10's to 1000's of picofarads). When designing with a MOV it is necessary to remember that as the current through the device increases, the voltage which the MOV clamps at is greatly increased.

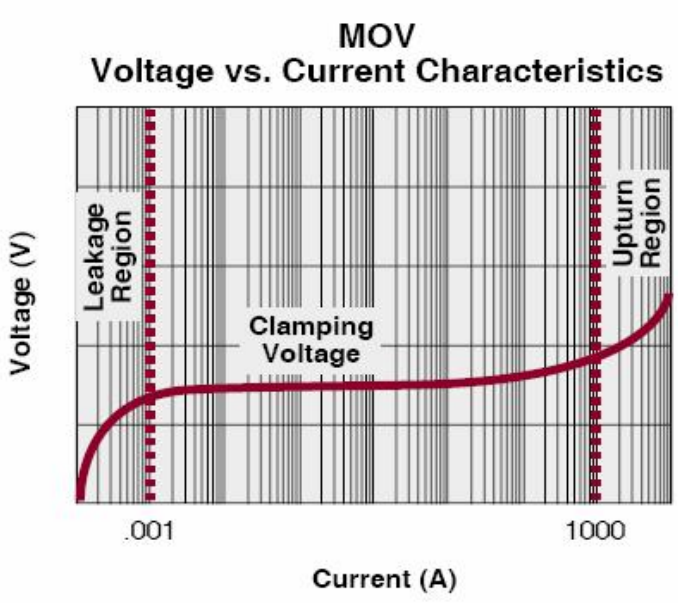


Figure 4

GDT and MOV PROTECTION

In summary, there is no one ideal surge arrester device type that meets all of the key performance parameters for every application. Due to their complementary performance characteristics, however, a GDT and MOV can be combined in a circuit to provide the ultimate in surge suppression performance. The MOV quickly clamps a fast rising voltage surge while the GDT crowbars to safely dissipate the large peak current to ground.

SUMMARIZED COMPARISON OF TECHNOLOGIES

	GAS TUBE CG2230L	SCR	MOV	DIODE
Type of Device	CROWBAR	CROWBAR	CLAMP	CLAMP
Response Speed	<1 uSEC.	<100nSEC.	<100nSEC.	<100nSEC.
Capacitance	1pF MAX.	50pF	45pF	50pF
Leakage Current	<1 pAMP	50 nAMPS	10,000 nAMPS	10,000 nAMPS
Maximum Surge Current (8/20 ☐sec wave form)	20,000 AMPS	500 AMPS	200AMPS	50 AMPS
Relative Cost	$1.00	$1.50	$0.50	$1.50

3.7.5 Application Note AN-112

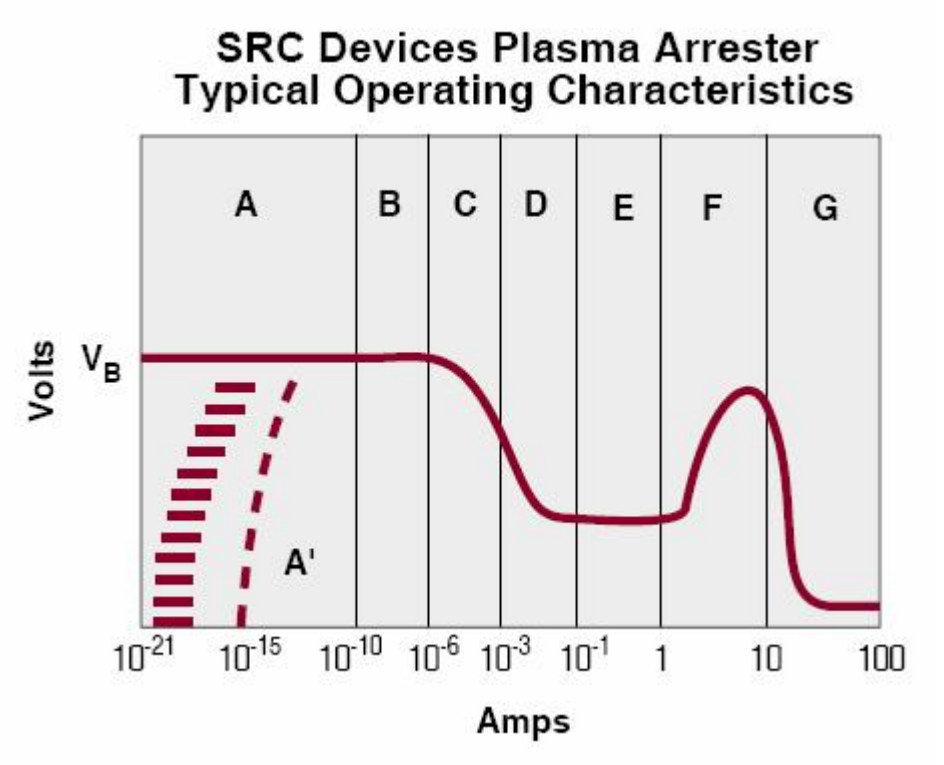
3.7.5.1 AN-112: Gas Discharge Tube (GDT) Theory

3.7.5.2 Construction

Gas Discharge Tube (GDT) surge arresters commonly employ hermetically-sealed enclosures utilizing either ceramic-to-metal or glass-to-metal seals. The many advantages of ceramic-to-metal units have made them the norm for gas discharge tube surge arresters such as those from SRC. Along with being low cost, they offer high product uniformity capable of handling extreme levels of shock, vibration, and temperature. The ceramic for GDT's is alumina ranging from 94- 98% Al2O3. The ceramic-to-metal seals are prepared by moly-manganese or tungsten metallizing processes with nickel plating and the final seal is made in a gasfilled vacuum furnace using braze preforms made of copper-silver eutectic. The electrodes used for GDT's are either copper or a nickel-iron alloy, often with a coating to lower the work function and/or add gettering capability. Stripes or bands of semi-conductive material are applied to the inner surfaces of the ceramic to improve stability and high-speed response.

3.7.5.3 Theory

The basic operation of gas tube surge arrestors such as SRC GDT's is best understood by referring to the schematic form of the voltage-current (V-i) relationship of a generic gas discharge device such as the one depicted in Figure 1.



Description of Regions of a Generic V-i Characteristic of a Plasma Device
Figure 1

A For voltages below the breakdown voltage, the gas provides a good insulator. Very low leakage currents (10-12A) occasionally encountered result from ionization by cosmic rays, high energy photons, etc; and is, therefore, subject to statistical fluctuations.
A1 The current is higher due to supplementary electron sources such as photoemission.
B The discharge is self-sustaining due to gas ionization –if external agents such as those mentioned for regions A and A1 are removed, the current will not change (Townsend discharge). This occurs at the breakdown voltage of the device.
C The transition region. As the electric field increases, more secondary electrons are generated, decreasing the voltage drop until the glow voltage (region D) is reached. Stable operation can only be maintained with active current regulation because of the negative slope of the V-i characteristic.
D The glow region (or normal glow region). In this region, the glow voltage is roughly constant with respect to small changes in current.
E The abnormal glow region. In contrast to the normal glow region, the glow voltage begins to increase as the current is increased.
F The glow-to-arc transition region.
G The arc region. In this region, the arc voltage will quickly drop and the arc current will quickly increase within the limitations of the drive energy and impedance.

If the current through the gas discharge device is adjusted over the range of values of 10-18 to 102 amps, the voltage across the device will also vary. When a gas discharge device is operated as a transient voltage protector, the modes of operation of greatest significance are in regions A, F, and G. The applied voltage is normally less than the breakdown voltage of the device, VBD, at which time the current through the device is in the A region. The charged carriers of electric current in this mode originate from the cathode by photon emission and within the fill gas by collisions of gas particles with cosmic rays (or radioactive decay particles if an isotope is used in the device). As soon as the applied voltage across the device exceeds the breakdown voltage, the current through the device increases rapidly to values of several amps or greater. The rate of current rise and the level reached is limited by the source capacity and the series impedance of the circuit. The voltage across the device at this time is very low with typical values of 20V or less.

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3.8 Estándares de seguridad eléctrica. (2.6)

3.8.1 IEC Electromagnetic Compatibility Standards.

3.8.1.1 For Industrial Process Measurement and Control Equipment

Application Note January 1998 **AN9734**

3.8.1.2 Introduction

The purpose of the **I**nternational **E**lectro-technical **C**ommission lEC 1000-4 (previously known as lEC-801) standard is to establish a common reference for evaluating the performance of industrial-process measurement and control instrumentation when exposed to electric or electromagnetic interference. The types of interference considered are those arising from sources external to the equipment.

The interference susceptibility tests are essentially designed to demonstrate the capability of equipment to function correctly when installed in its working environment. The type of test required should be determined on the basis of the interference to which the equipment may be exposed when installed while taking into consideration the electrical circuit (i.e., the way the circuit and shields are tied to earth ground), the quality of shielding applied, and the environment in which the system is required to work.

The lEC 1000-4 standard is divided into six sections:

lEC 1000-4-1. Introduction
lEC 1000-4-2. Electrostatic Discharge Requirements
lEC 1000-4-3. Radiated Electromagnetic Field Requirements
lEC 1000-4-4. Electrical Fast Transient (Burst) Requirements
lEC 1000-4-5. Surge Voltage Immunity Requirements
lEC 1000-4-6. Immunity to Conducted Disturbances Induced by Radio Frequency Fields Above 9kHz

Sections lEC 1000-4-2 through lEC 1000-4-5 will be discussed in this application note.

TEST SEVERITY LEVEL

LEVEL	TEST VOLTAGE: CONTACT DISCHARGE	TEST VOLTAGE: AIR DISCHARGE
1	2kV	2kV
2	4kV	4kV
3	6kV	8kV
4	8kV	15kV
X	Special	Special

NOTES:
1. "X" is an open level.
2. The test severity levels shall be selected in accordance with the most realistic installation and environmental conditions.

CHARACTERISTICS OF THE ESD GENERATOR

LEVEL	INDICATED VOLTAGE	FIRST PEAK CURRENT OF DISCHARGE (±±10%)	RISE TIME WITH DISCHARGE SWITCH	CURRENT AT 30ns (±30%)	CURRENT AT 60ns (±30%)
1	2kV	7.5A	0.7 to 1ns	4A	2A
2	4kV	15A	0.7 to 1ns	8A	4A
3	6kV	22.5A	0.7 to 1ns	12A	6A
4	8kV	30A	0.7 to 1ns	16A	8A

3.8.1.3 Electrostatic Discharge (ESD) Requirements

The purpose of this test is to find the reaction of the equipment when subjected to electrostatic discharges which may occur from personnel to objects near vital instrumentation.
In order to test the equipment's susceptibility to ESD, the test setup conditions must be established. Direct and indirect application of discharges to the Equipment Under Test (EUT) are possible, in the following manner:

a) Contact discharges to the conductive surfaces and to coupling planes.
b) Air discharge at insulating surfaces.

Two different types of tests can be conducted:

1. Type (conformance) tests performed in laboratories.
2. Post installation tests performed on equipment in its installed conditions.

The only accepted method of demonstrating conformance to the standard is the of type tests performed in laboratories.
The EUT, however, shall be arranged as closely as possible to the actual installation conditions.
Examples of laboratory ESD test setups can be seen in Figure 1 for tabletop equipment and in Figure 2 for floor standing equipment.
Post installation tests are optional and not mandatory for certification. If a manufacturer and customer agree post installation tests are required, a typical test setup can be found in Figure 3.

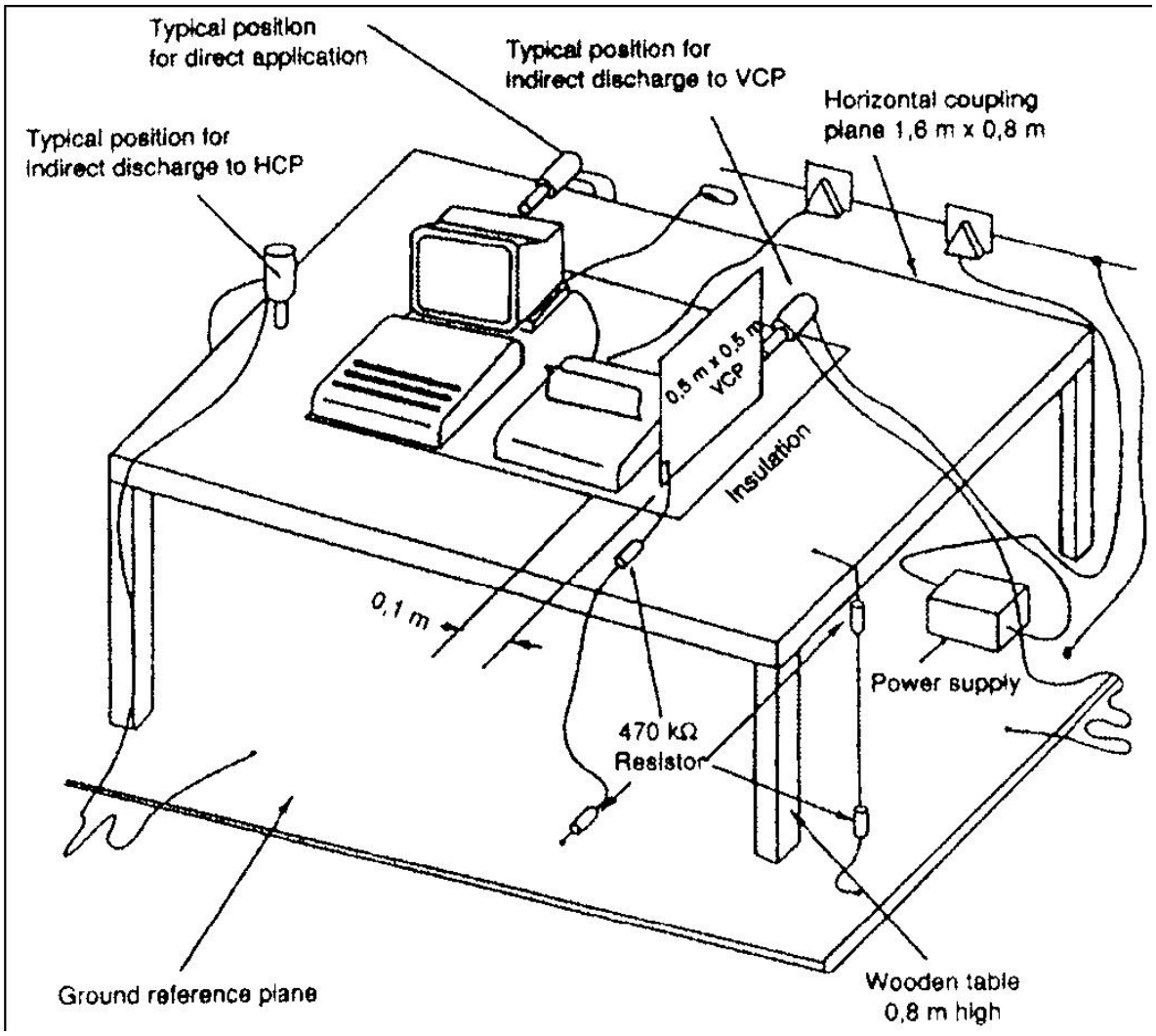


FIGURE 1. EXAMPLE OF TEST SETUP FOR TABLETOP EQUIPMENT, LABORATORY TESTS

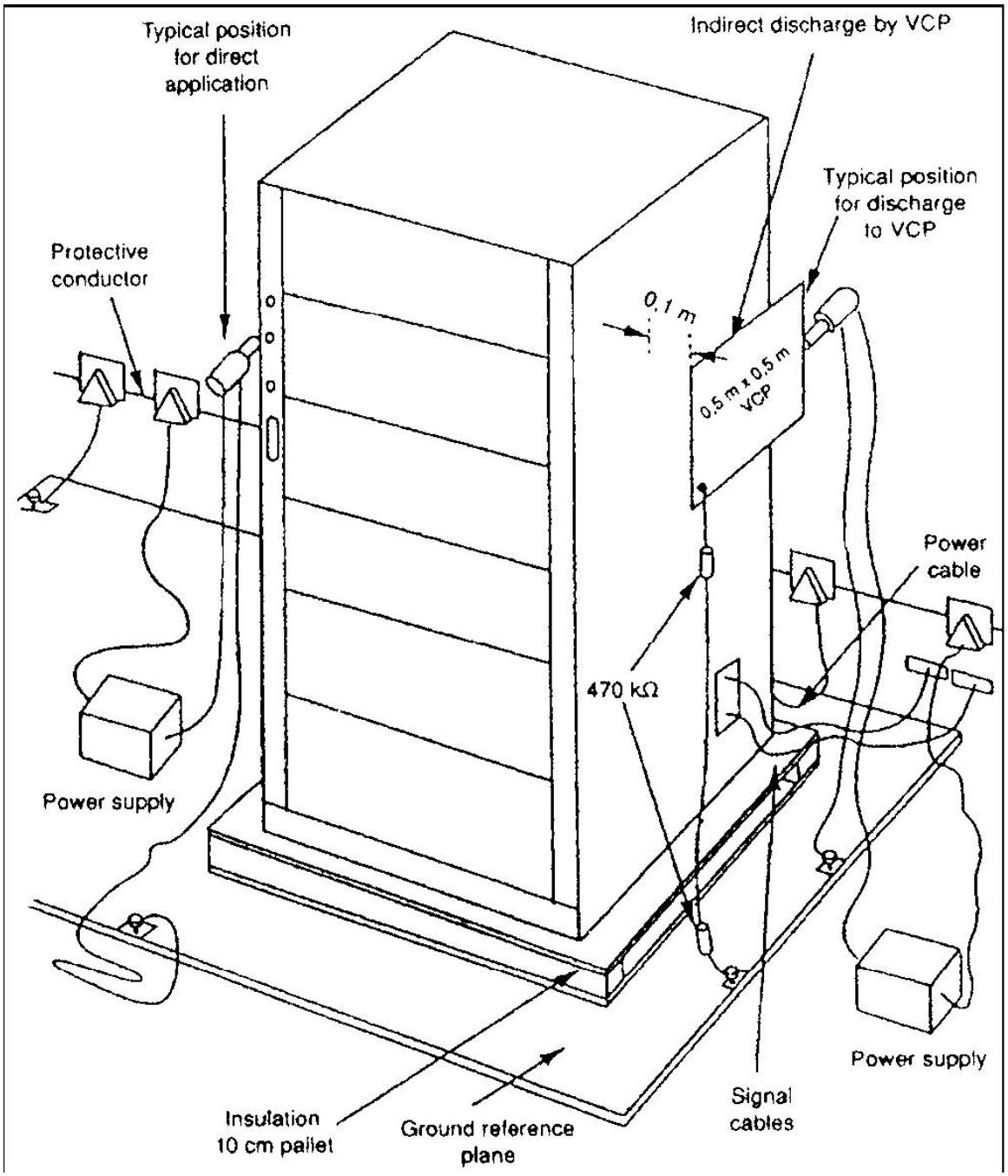


FIGURE 2. EXAMPLE OF TEST SETUP FOR FLOOR STANDING EQUIPMENT, LABORATORY TESTS

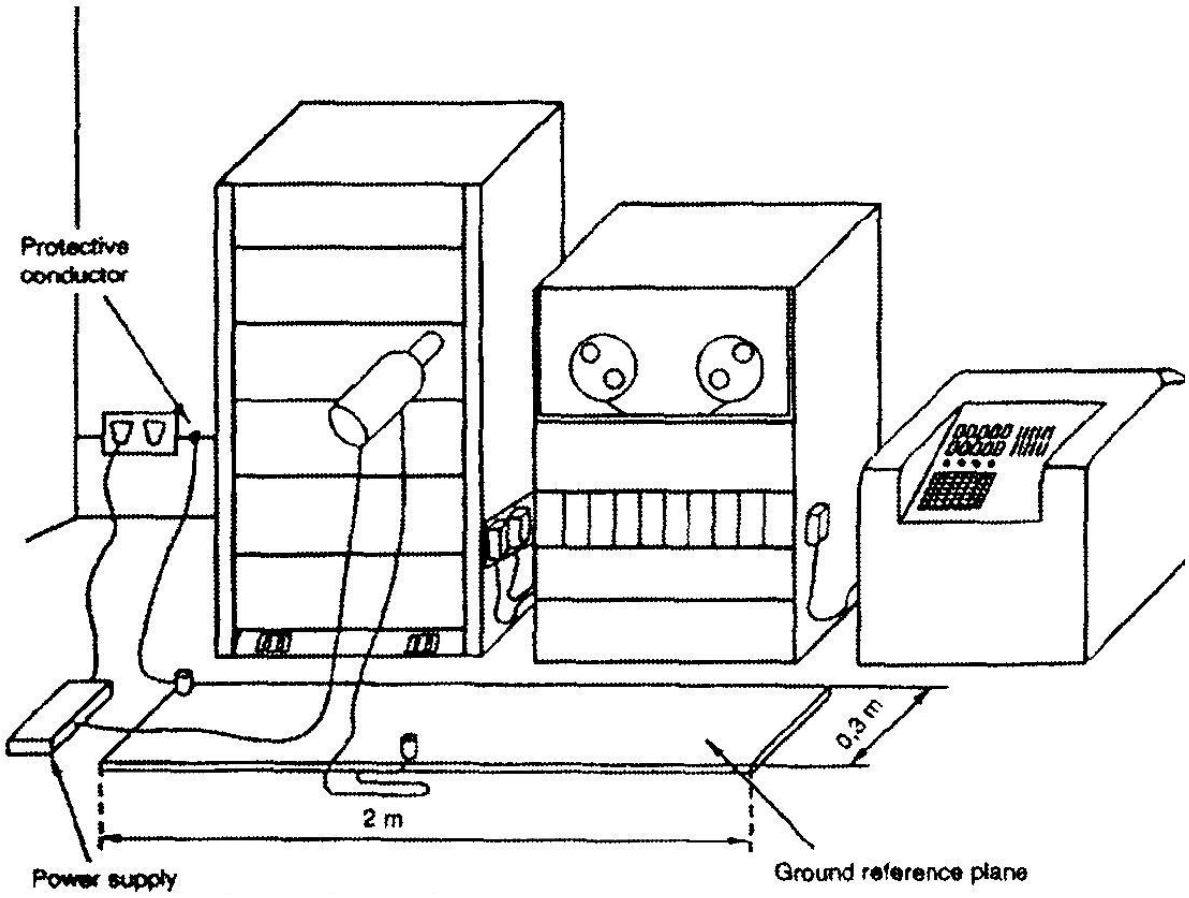


FIGURE 3. EXAMPLE OF TEST SETUP FOR EQUIPMENT, POST-INSTALLATION TESTS

Test Procedure

• For conformance testing, the EUT shall be continually operated in its most sensitive mode which shall be determined by preliminary testing.
• The test voltage shall be increased from the minimum to the selected test severity level.
• Number: at least 10 single discharges (in the most sensitive polarity).
• Time interval: initial value 1 second, longer intervals may be necessary.
• Direct application of discharge to the EUT: The static electricity discharges shall be applied only to those points and surfaces of the EUT which are accessible to the human operator during normal usage.
• Indirect application of the discharge: Discharges to objects placed or installed near the EUT shall be simulated by applying the discharges to a coupling plane (a horizontal coupling plane under the EUT or a vertical coupling plane).

Test Results

The results of the ESD tests are reported as follows:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of date.

3.8.1.4 IEC 1000-4-3 Radiated Electromagnetic Field Requirements

This test shows the susceptibility of instrumentation when subjected to electromagnetic fields such as those generated by portable radio transceivers or any other device that will generate continuous wave (CW) radiated electromagnetic energy.

TEST SEVERITY LEVELS

Frequency band: 27MHz to 500MHz

LEVEL	TEST FIELD STRENGTH (V/M)
1	1
2	3
3	10
X	Special

NOTES:
3. "X" is an open class.
4. The test severity levels shall be selected in accordance with the electromagnetic radiation environment to which the EUT may be exposed when finally installed.

Test Setup

Examples of the test configuration for radiated electromagnetic fields can be found in Figure 4 and Figure 5.

- The procedure requires the generation of electromagnetic fields within which the test sample is placed and its operation observed. The tests shall be carried out in a shielded enclosure or anechoic chamber The test procedure assumes the use of biconical and log-spiral antennae or stripline.
- All testing of the equipment shall be performed in conditions as close as possible to the actual installation. Small objects (25cm x 25cm x 25cm) can be tested using a stripline antennae. This is a parallel plate transmission line to generate an electromagnetic field as shown in Figure 6.

Test Procedure

• The test is performed with the EUT in the most sensitive physical orientation.
• The frequency range is swept from 27 MHz to 500 MHz. The sweep rate is in the order of 1.5 x 10-3 decades/s.

Test Results

The results of the radiated electromagnetic field include:
• The effect of the electromagnetic field on the output of the EUT
- As a consistent measurable effect.
- As a random effect, not repeatable, and possibly further classified as a transient effect occurring during the application of the electromagnetic field and as a permanent or semipermanent field after the application of the electromagnetic field.
• Any damage to the EUT resulting from the application of the electromagnetic field. The qualitative evaluation of the resultant data needs to be assessed in terms of the existing local ambient electromagnetic level and the specific operating frequencies.

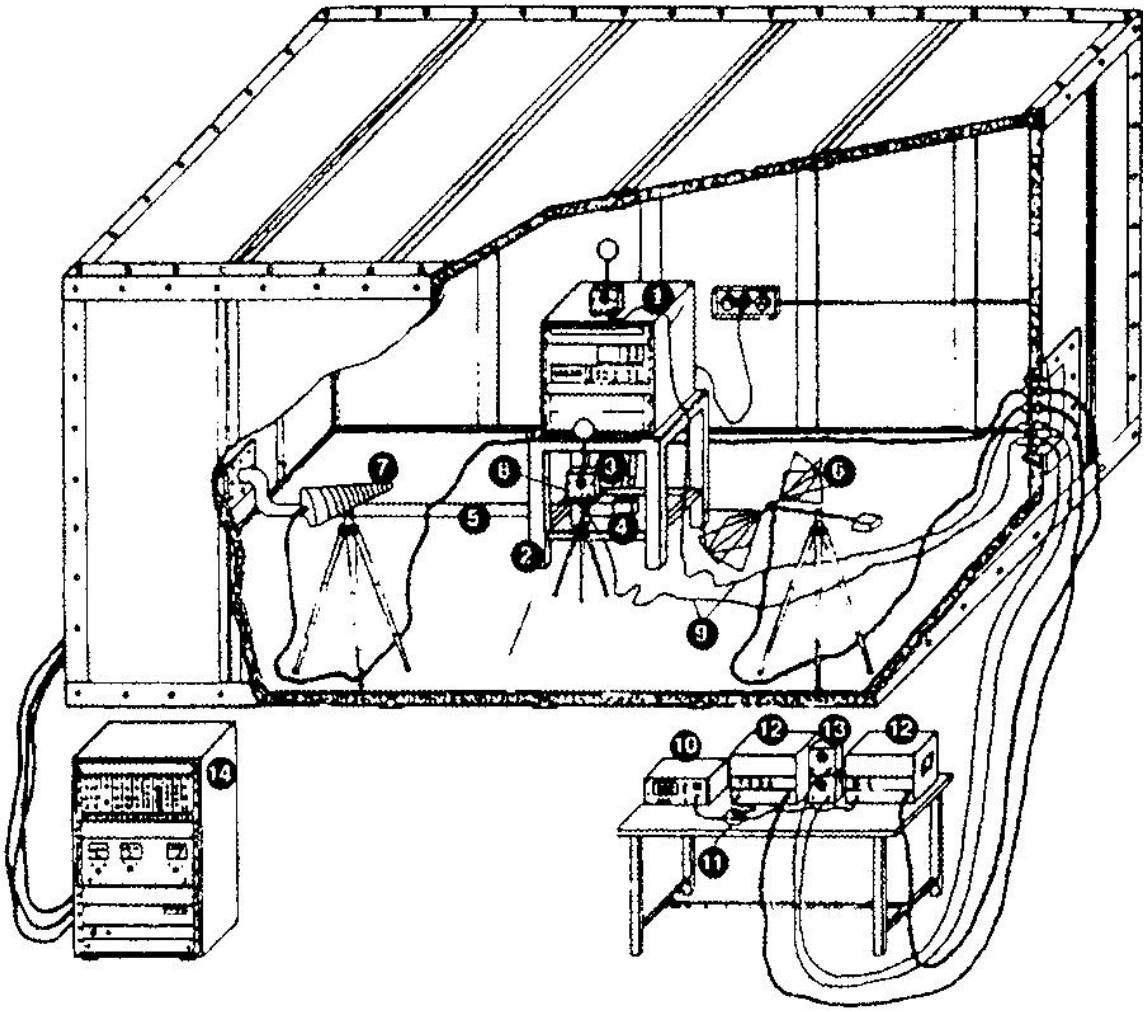


FIGURE 4. TEST SETUP FOR RADIATED ELECTROMAGNETIC FIELD TESTS IN A SHIELDED ROOM WHERE THE ANTENNAE, FIELD STRENGTH MONITORS AND EUT ARE INSIDE AND THE MEASURING INSTRUMENTS AND ASSOCIATED EQUIPMENT ARE OUTSIDE THE SHIELDED ROOM

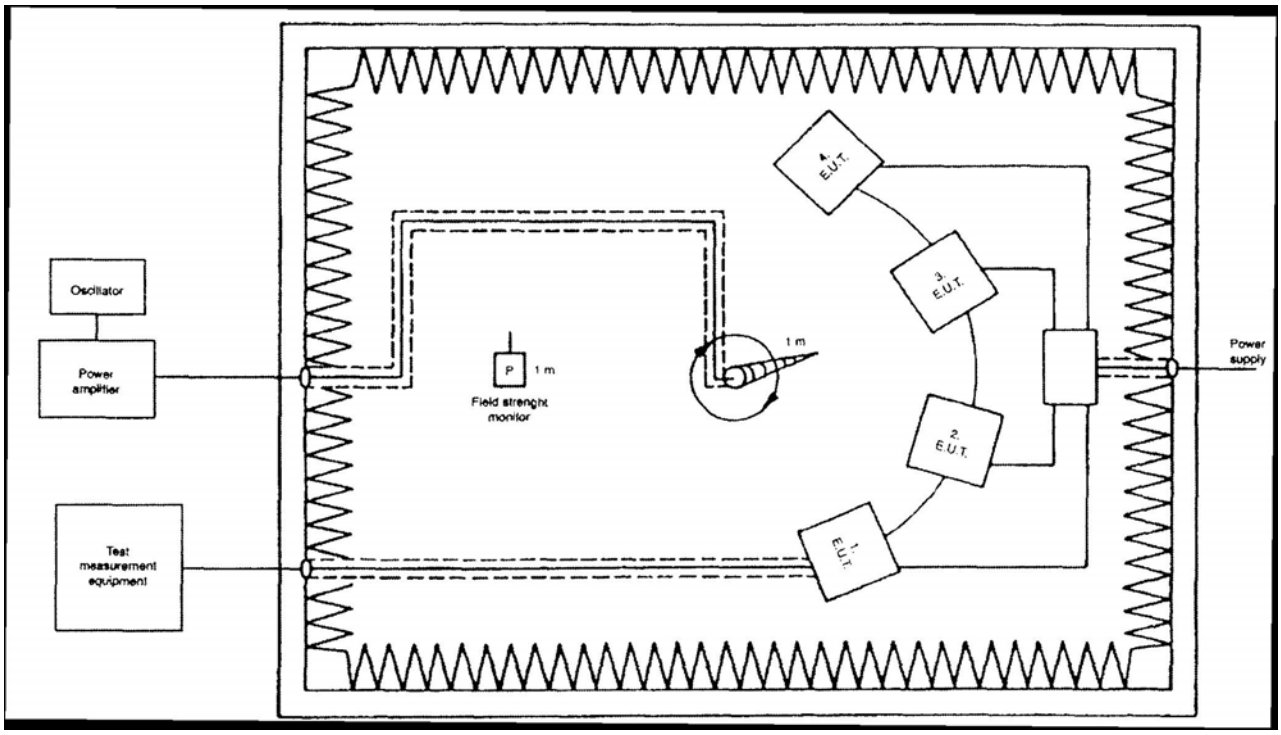


FIGURE 5. TEST SETUP FOR RADIATED ELECTROMAGNETIC FIELD TESTS IN AN ANECHOIC CHAMBER, GENERAL ARRANGEMENT OF THE EUT, FIELD STRENGTH MONITOR AND ANTENNAE

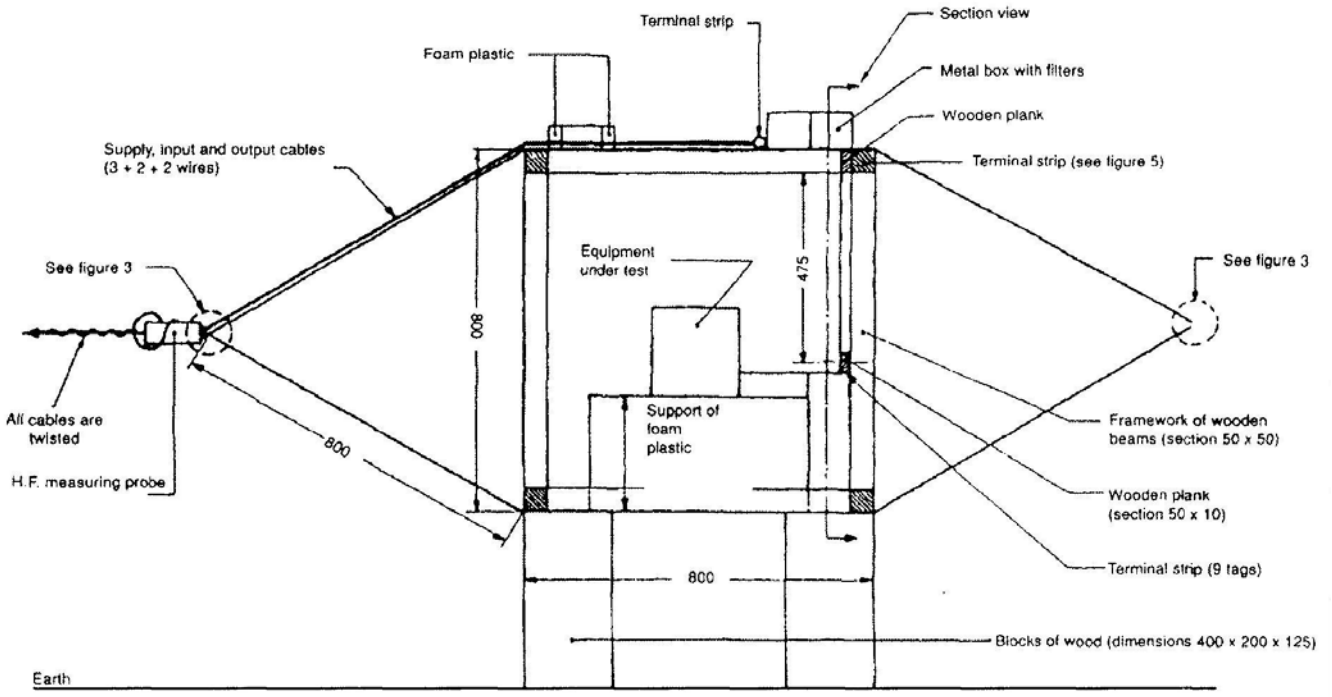


FIGURE 6. TEST SETUP WITH STRIPLINE CIRCUIT

3.8.1.5 IEC 1000-4-4 Electrical Fast Transient (Burst) Requirements

This test is intended to demonstrate the immunity of the equipment when subjected to interference originating from switching transients.

TEST SEVERITY LEVELS

Open circuit output test voltage:

LEVEL	ON POWER SUPPLY	ON INPUT/OUTPUT SIGNAL DATA AND CONTROL LINES
1	0.5kV	0.25kV
2	1kV	0.5kV
3	2kV	1kV
4	4kV	2kV
X	Special	Special

NOTES:
5. "X" is an open level.
6. The test severity levels shall be selected in accordance with the most realistic installation and environmental conditions.

Characteristics of the Fast Transient/Burst Generator

- Rise time of one pulse: 5ns ± 30%
- Impulse duration (50% value): 50ns ± 30%
- Repetition rate of the impulses and peak values of the output voltage: 5kHz ☐} 20% at 0.125kV 5kHz ☐} 20% at 0.25kV 5kHz ☐} 20% at 0.5kV 5kHz ☐} 20% at 1.0kV 5kHz ☐} 20% at 2.0kV
- Burst duration: 15ms ☐} 20%
- Burst period: 300ms ☐} 20%

Test Setup

For laboratory testing, the test setup for type testing can be shown in Figure 7 and Figure 8.

- Power supply lines (See Figure 7): If the line current is higher than 100A, the "field test" shall be used.
- Earth connections of the cabinets: The test point on the cabinet shall be the terminal for the protective earth conductor (See Figure 7).
- Input/Output circuits and communication lines (See Figure 8).

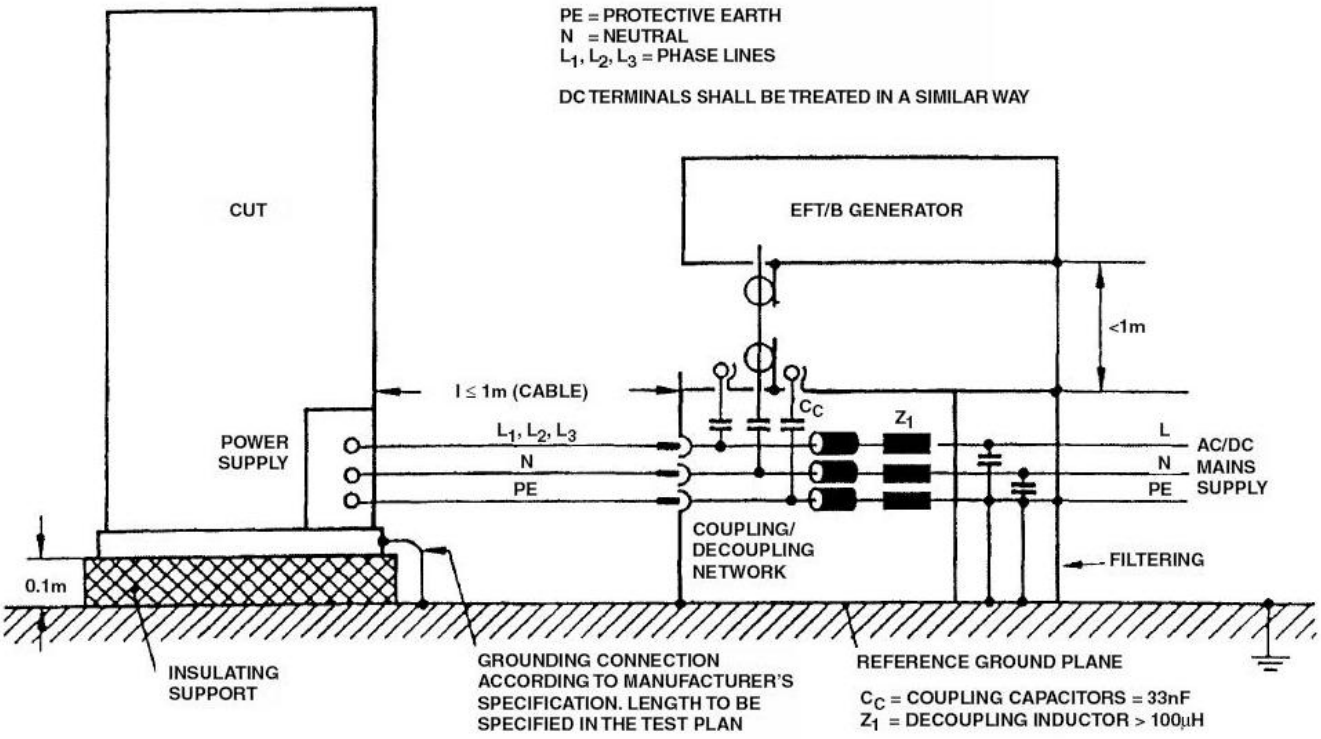


FIGURE 7. EXAMPLE OF TEST SETUP FOR DIRECT COUPLING OF THE TEST VOLTAGE TO AC/DC POWER SUPPLY LINES/TERMINALS FOR LABORATORY TEST PURPOSES

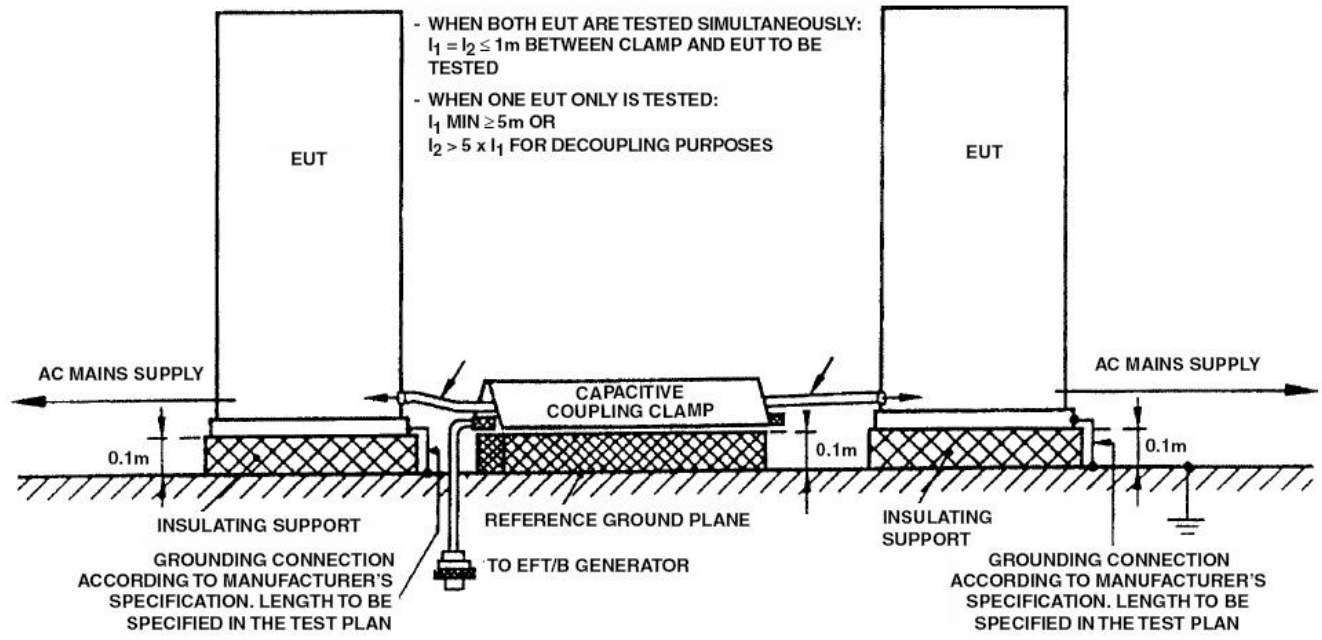


FIGURE 8. EXAMPLE OF TEST SETUP FOR APPLICATION OF THE TEST VOLTAGE BY THE CAPACITIVE COUPLING CLAMP FOR LABORATORY TEST PURPOSES

3.8.1.6 IEC 1000-4-4 Electrical Fast Transient (Burst) Requirements

For field testing, the equipment or system shall be tested in the final installed conditions without coupling/decoupling networks.

• Power supply lines and protective earth terminals

- Stationary, floor-mounted EUT: The test voltage shall be applied between a reference ground plane and each of the power supply terminals, AC or DC, and on the terminals for the protective or function earth on the cabinet of the EUT. (See Figure 9).

- Non-stationary mounted EUT, connected to the mains supply by flexible cord and plugs: The test voltage shall be applied between each of the power supply conductors and the protective earth at the power supply outlet to which the EUT is to be connected. (See Figure 10).

• Input/Output circuits and communication lines:

- A capacitive clamp shall be used for coupling the test voltage into the lines. However, if the clamp cannot be used due to mechanical problems in the cabling, it may be replaced by a tape or a conductive foil enveloping the lines under test. (See Figure 11).

Test Procedure

• Polarity of the test voltage: both polarities are mandatory

• Duration of the test: at least 1 minute

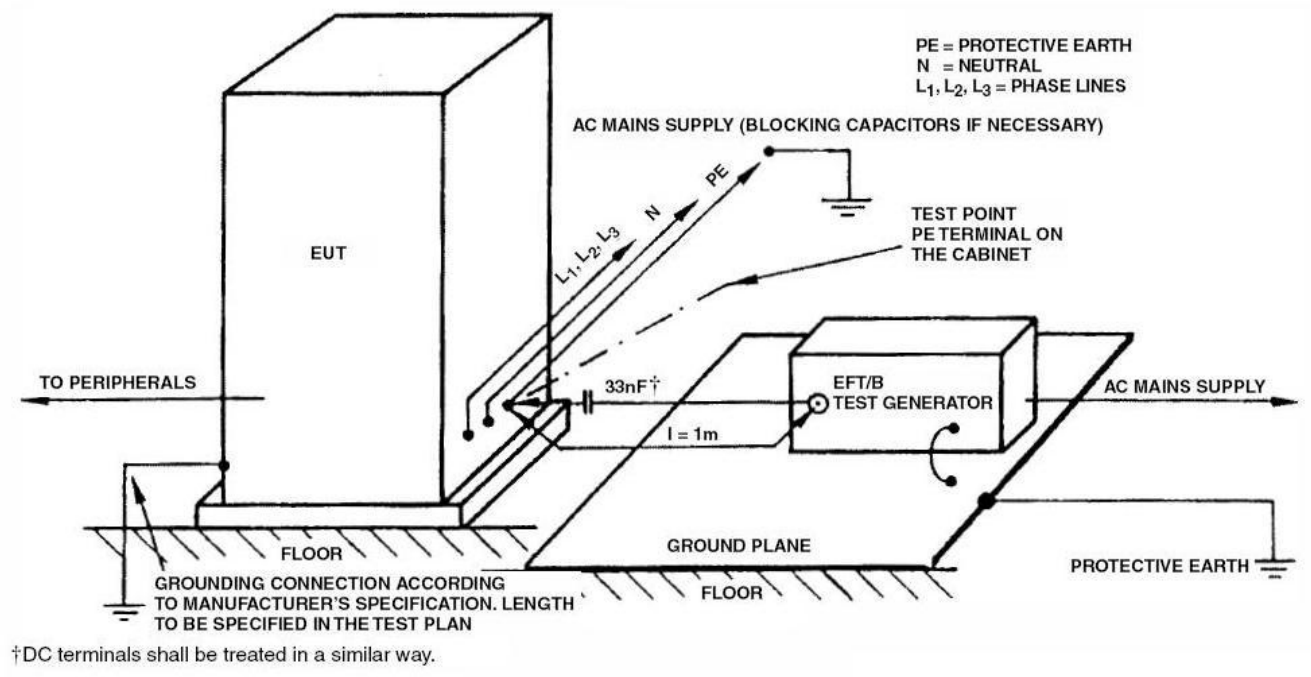


FIGURE 9. EXAMPLE OF FIELD TEST ON AC/DC POWER SUPPLY LINES AND PROTECTIVE EARTH TERMINALS FOR STATIONARY, FLOOR MOUNTED EUT

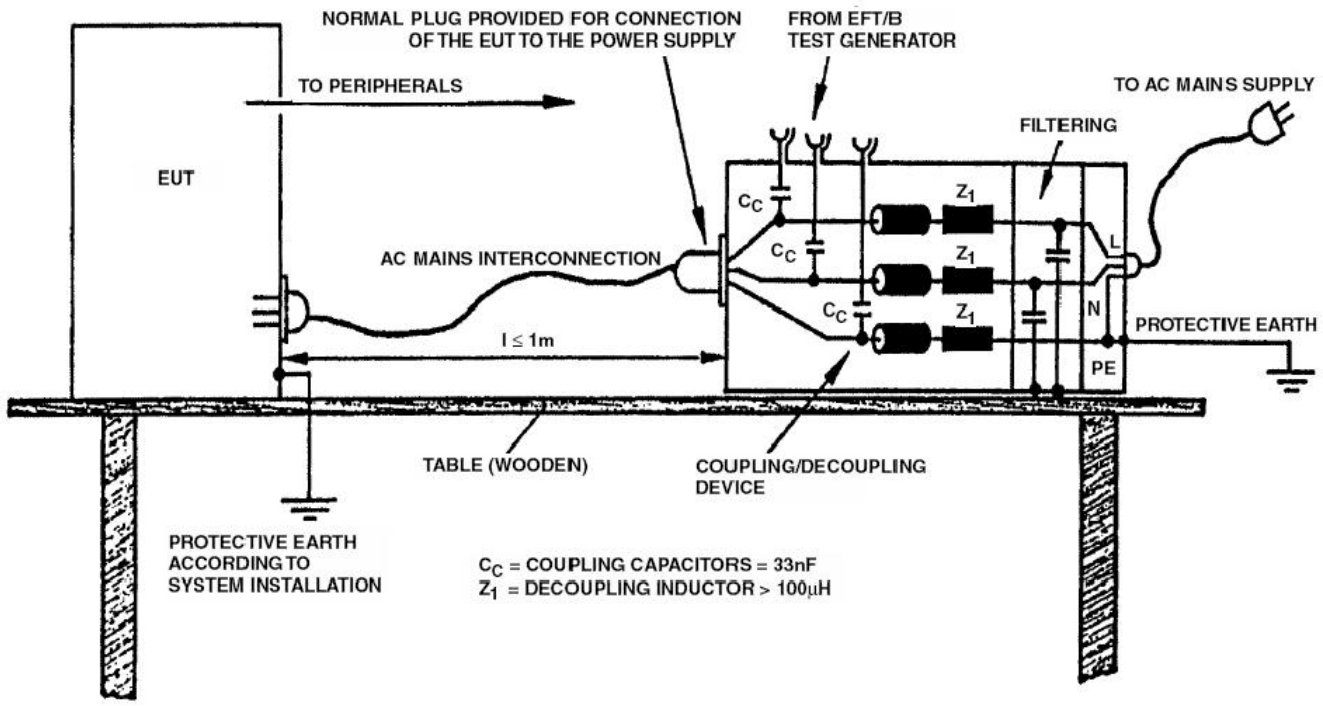


FIGURE 10. EXAMPLE OF FIELD TEST ON AC MAINS SUPPLY AND PROTECTIVE EARTH TERMINALS FOR NON-STATIONARY MOUNTED EUT

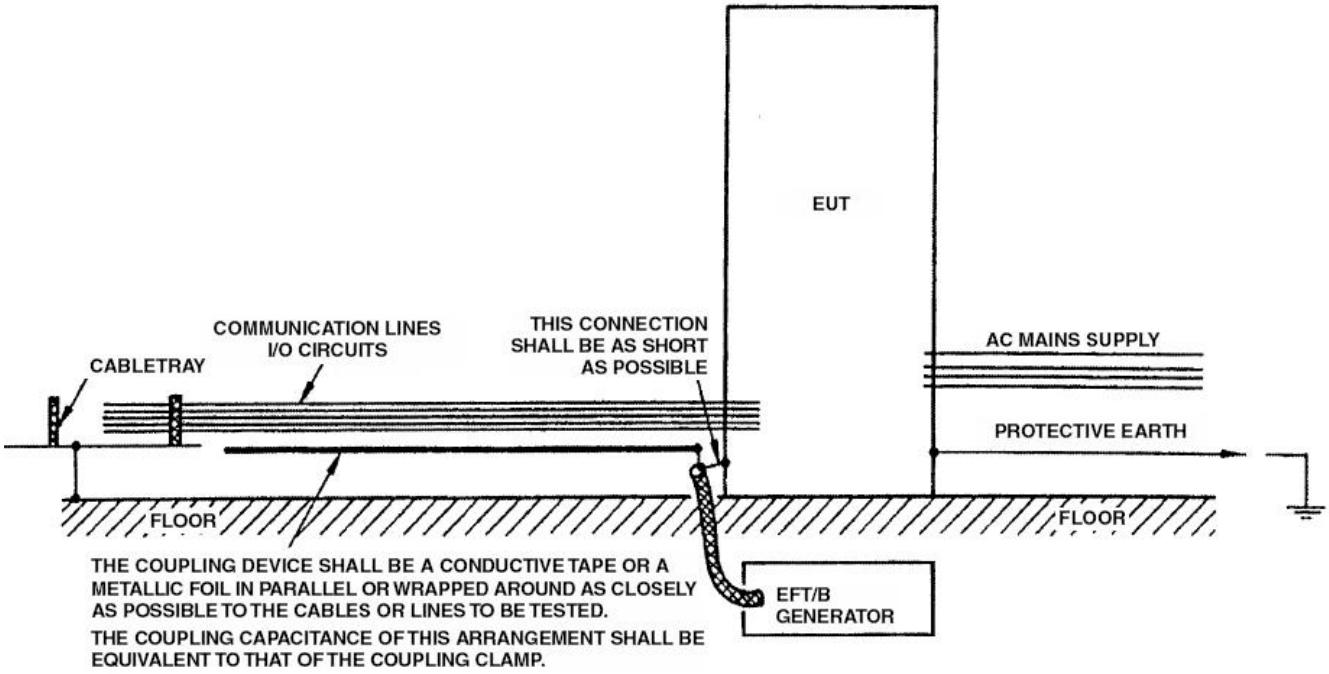


FIGURE 11. EXAMPLE OF FIELD TEST ON COMMUNICATIONS AND I/O CIRCUITS WITHOUT THE CAPACITIVE COUPLING CLAMP

Test Results

The results are reported as:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of data.

3.8.1.7 IEC 1000-4-5 Surge Voltage Immunity Requirements

The goal of the laboratory test is to determine the equipment's susceptibility to damage caused by overvoltage surges caused by circuit switching and lightning strikes.

TEST SEVERITY LEVELS

CLASS	POWER SUPPLY		UNSYM LINES LONG DATA BUS		SYMMETRICAL LINES	DATA BUS SHORT (DIST)
	LINE TO LINE Z = 2	LINE TO GROUND Z = 12	LINE TO LINE Z = 42	LINE TO GROUND Z = 42	LINE TO GROUND Z = 42	LINE TO GROUND
0	No Test is Advised					
1	-	0.5kV	-	0.5kV	1.0kV	-
2	0.5kV	1.0kV	0.5kV	1.0kV	1.0kV	0.5kV
3	1.0kV	2.0kV	1.0kV	2.0kV	2.0kV	-
4	2.0kV	4.0kV	2.0kV	4.0kV	-	-
5	(Note 8)	(Note 8)	2.0kV	4.0kV	4.0kV	-
X	Special					

NOTES:

7. Z is the source impedance.
8. Depends on the class of the local power supply system. "X" is an open level that has to be specified in the product specification. The class depends on the installation conditions.

Characteristics of the Test Instrumentation

• Combination wave test generator
- Open circuit output voltage . . . . . 0.5kV to 4.0kV
- Short circuit output current . . . . . 0.25kA to 2.0kA

• Test generator 10/700µs (according to CCITT):
- Open circuit output voltage . . . . . 0.5kV to 4.0kV
- Short circuit output current . . . . . 12.5A to 100A

	IN ACCORDANCE WITH IEC60-2		IN ACCORDANCE WITH IEC469-1	
	FRONT TIME	TIME TO HALF VALUE	RISE TIME (10%-90%)	DURATION (50%-50%)
Open Circuit Voltage	1.2µs	50µs	1µs	50µs
Short Circuit Current	8µs	20µs	6.4µs	16µs

	IN ACCORDANCE WITH IEC60-2		IN ACCORDANCE WITH IEC469-1	
	FRONT TIME	TIME TO HALF VALUE	RISE TIME (10%-90%)	DURATION (50%-50%)
Open Circuit Voltage	10µs	700µs	6.5µs	700µs
Short Circuit Current	-	-	4µs	300µs

NOTE: The surges (and test generators) related to the different classes are:
Class 1 to 4: 1.2/50µs (8/20µs)
Class 5: 1.2/50µs (8/20ms) and 10/700µs

NOTE: The surges (and test generators) related to the different classes are:
Class 1 to 4: 1.2/50 µs (8/20µs)
Class 5: 1.2/50 µs (8/20ms) and 10/700 µs

Test Setup

A decoupling network is used to prevent surge energy from being propagated to the other equipment operating from the same source during testing of the EUT. The test setup for evaluating the EUT power supply is shown in Figures 12 - 15. A capacitive coupling network (preferred) or an inductive coupling network is used for this test. The test setup for evaluating the unshielded interconnection lines of the EUT is illustrated in Figures 16-20. Usually, capacitive coupling is used, but inductive coupling or coupling via gas discharge tube (GDT) surge arrestors is also possible.

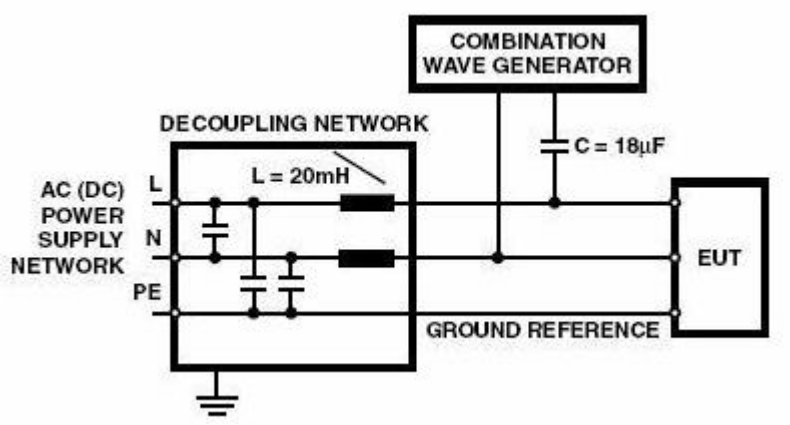


FIGURE 12. TEST SETUP FOR CAPACITIVE COUPLING ON AC/DC LINES; LINE TO LINE COUPLING ACCORDING TO 7.2

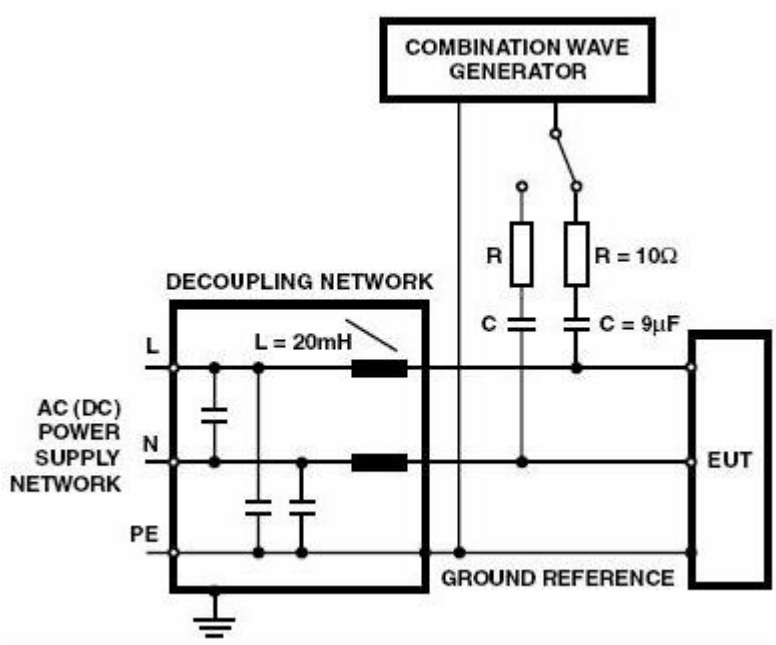


FIGURE 13. TEST SETUP FOR CAPACITIVE COUPLING ON AC/DC LINES; LINE TO GROUND COUPLING ACCORDING TO 7.2 (GENERATOR OUTPUT FLOATING OR EARTHED)

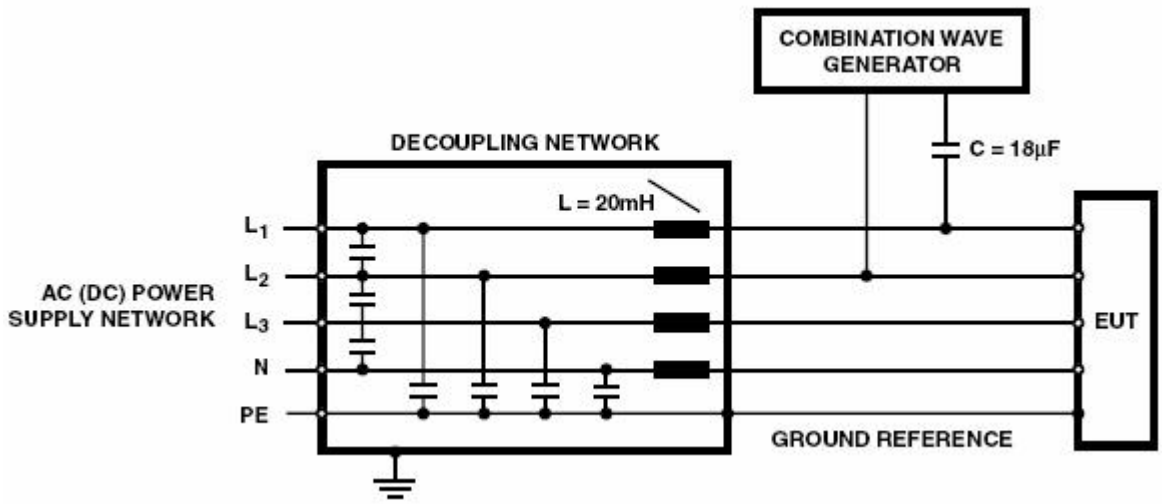


FIGURE 14. TEST SETUP FOR CAPACITIVE COUPLING ON AC LINES (3 PHASES); LINE TO LINE COUPLING ACCORDING TO 7.2

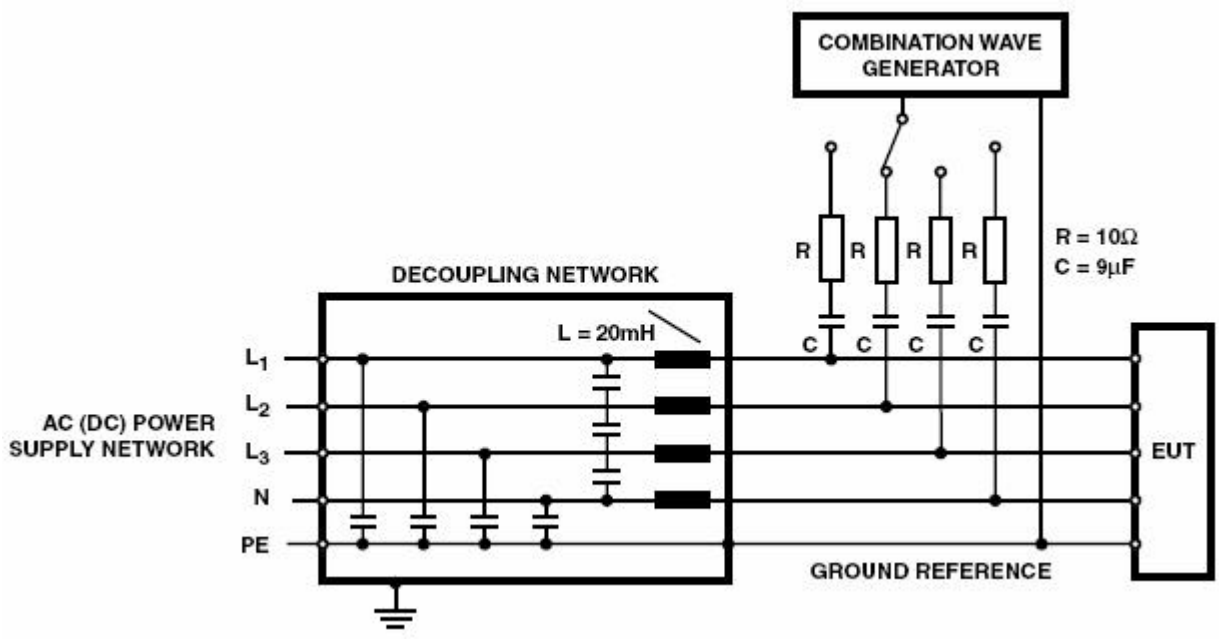


FIGURE 15. TEST SETUP FOR CAPACITIVE COUPLING ON AC LINES (3 PHASES); LINE TO GROUND COUPLING ACCORDING TO 7.2

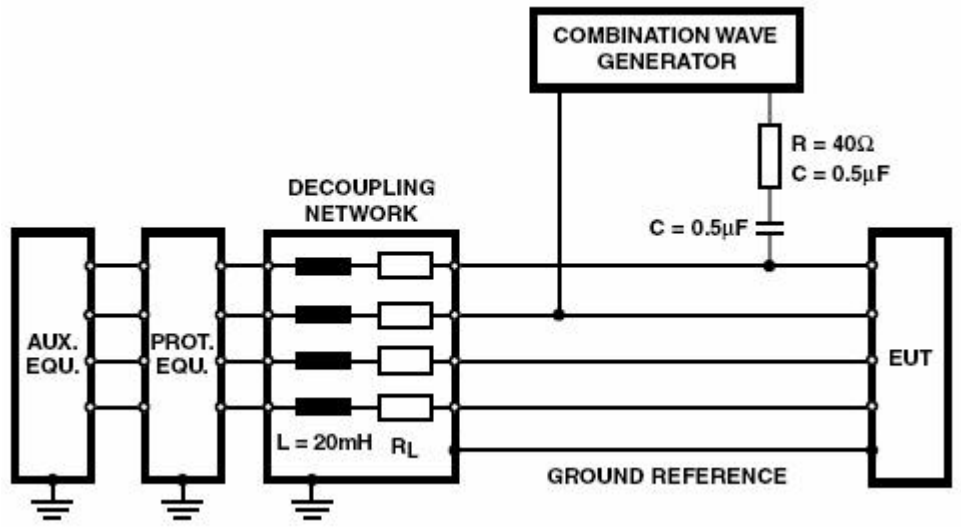


FIGURE 16. TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO LINE COUPLING ACCORDING TO 7.3; COUPLING VIA CAPACITORS

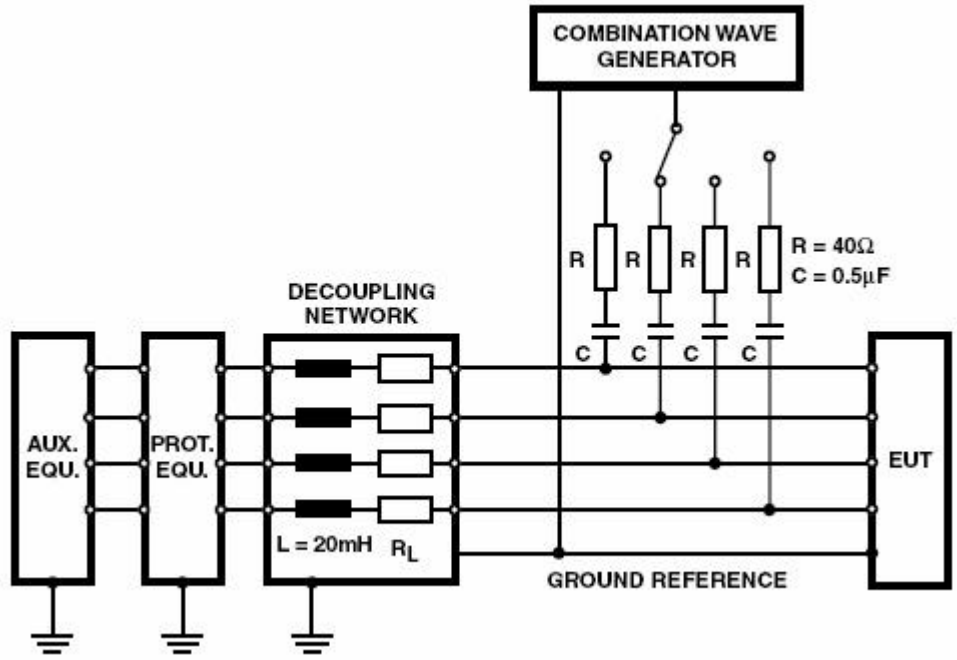


FIGURE 17. TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO GROUND COUPLING TO 7.3; COUPLING VIA CAPACITORS

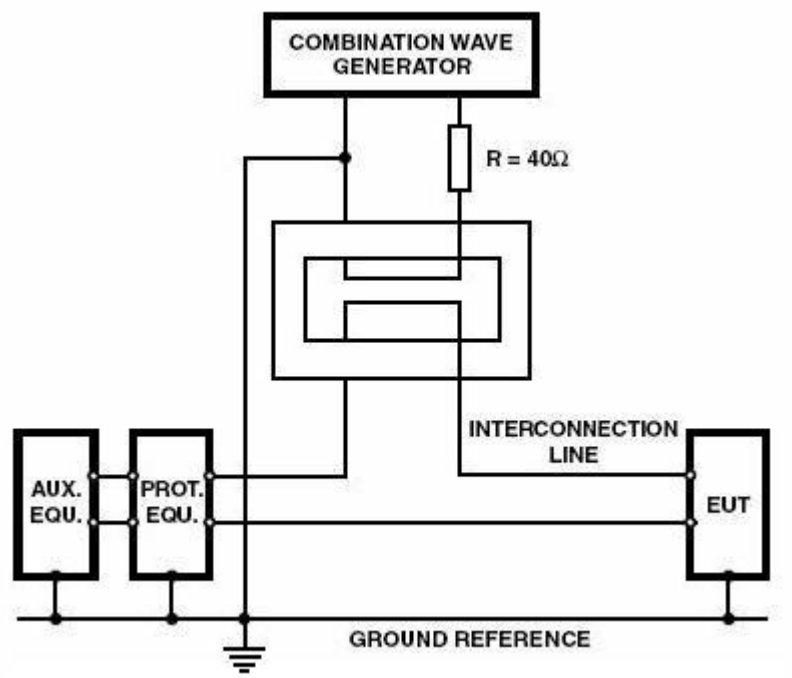


FIGURE 18. TEST SETUP FOR UNSHEILDED INTERCONNECTION LINES; LINE TO LINE COUPLING ACCORDING TO 7.3; INDUCTIVE COUPLING FOR HIGH IMPEDANCE CIRCUITS

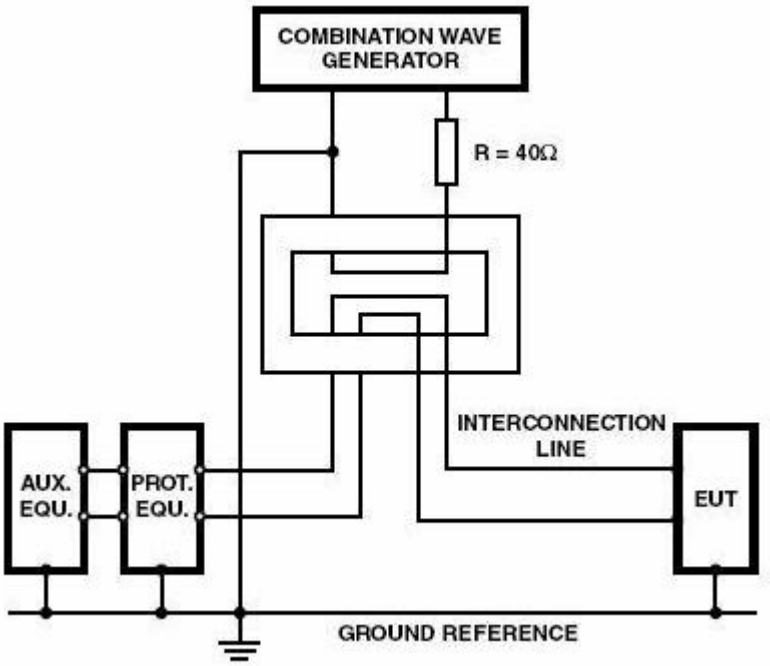


FIGURE 19. SIMPLIFIED TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO GROUND COUPLING ACCORDING TO 7.3; INDUCTIVE COUPLING FOR LOW IMPEDANCE CIRCUITS

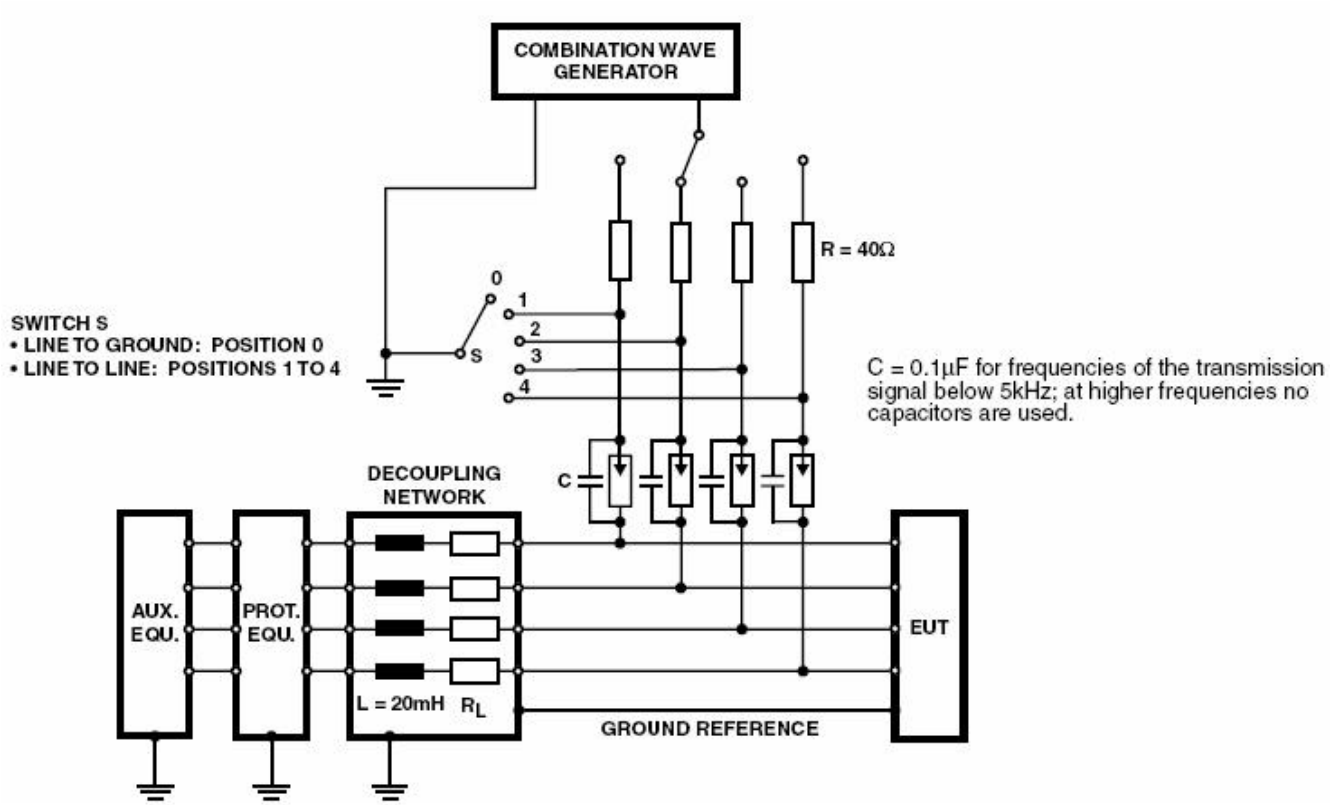


FIGURE 20. TEST SETUP FOR UNSHIELDED UNSYMMETRICALLY OPERATED LINES; LINE TO GROUND COUPLING ACCORDING TO 7.3; COUPLING VIA GAS ARRESTORS

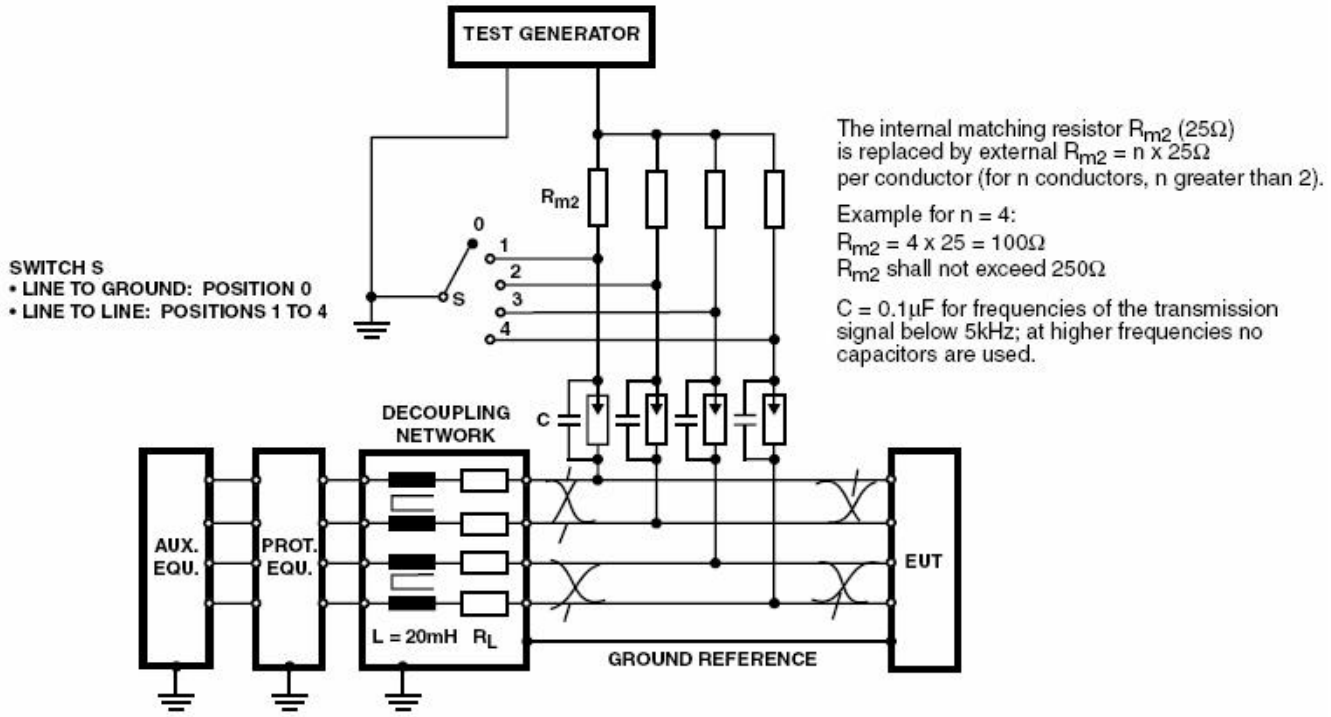


FIGURE 21. TEST SETUP FOR UNSHIELDED SYMMETRY OPERATED LINES (TELECOMMUNICATION LINES); LINE TO GROUND COUPLING ACCORDING TO 7.4; COUPLING VIA GAS ARRESTORS

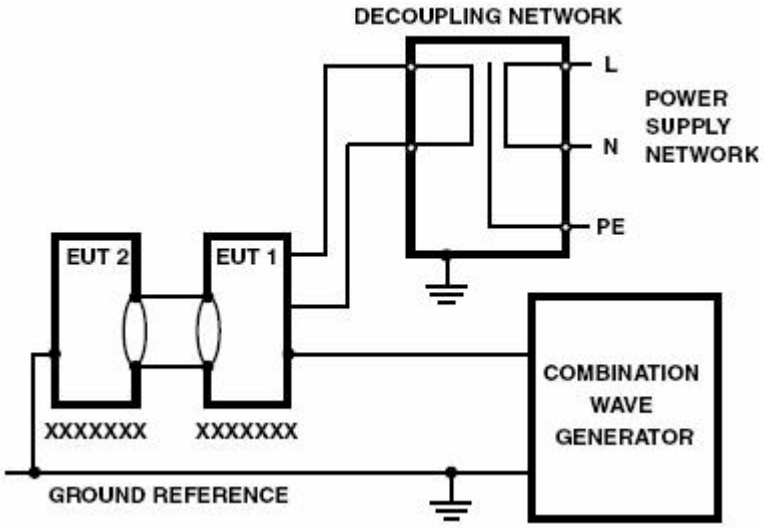


FIGURE 22. TEST SETUP FOR TESTS APPLIED TO SHIELDED LINES AND TO APPLY POTENTIAL DIFFERENCES ACCORDING TO 7.5 AND 7.6; GALVANIC COUPLING

Test Procedure

• Number of tests: at least 5 positive and 5 negative at the selected points.
• Pulse repetition: Max. 1/min.
• The maximum repetition rate depends on the built-in protection devices of the EUT.
• The surge will be applied between lines and between lines and ground.
• All lower levels including the selected test level must be satisfied. For testing the secondary protection, the output voltage of the generator must be increased up to the worst case voltage break down of the primary protection.

Test Results

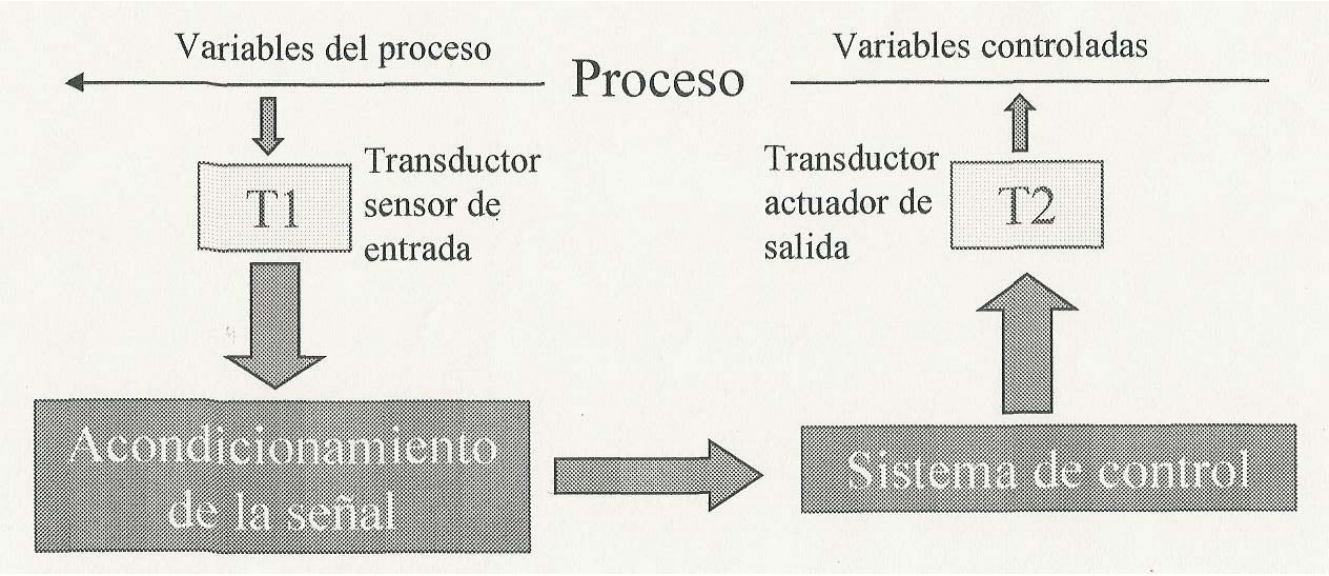
The results of the test are reported as follows:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of data.

4 UNIDAD 3. Acondicionamiento de señales.

4.1 Acondicionamiento de señal (I)

• Elemento o elementos de un sistema de medida o control que procesan la señal procedente de un transductor bien para adecuarla a un nuevo formato, bien para mejorar su *calidad.*



4.2 Acondicionamiento de señal (II) clasificación

4.2.1 • Cambios en niveles de señal

- • Amplificación.
- • Atenuación.
- • Eliminación de *offset*

4.2.2 • Linealización.

4.2.3 • Interfase digital

- • Multiplexores.
- • Muestreo y mantenimiento.
- • Conversión A/D.
- • Conversión D/A.

4.2.4 • Filtrado y ajuste de impedancia.

4.2.5 • Conversiones de señales

- • Conversión corriente/presión.
- • Puente de Wheatstone

4.2.6 • Transmisión de señal

- • Conversión tensión/corriente.
- • Conversión corriente/tensión.
- • Conversión tensión/frecuencia.
- • Modulación.

4.3 Acondicionamiento de señal (III)

Dos formas de implementación

- Analógica
  - **Circuitos pasivos (con resistencias, condensadores y bobinas).**
  - **Circuitos activos (con Amplificadores operacionales).**
  - **Menor coste.**
  - **Menor tiempo de procesado.**
- Digital
  - **Menor incertidumbre (menor influencia de ruidos, impedancias, etc.).**
  - **Rápido aumento del uso de computadores para medida y control.**
  - **Posibilidad de implementar procesamientos más comlejos.**
  - **Siempre es necesario un primer procesado analógico aun cuando la mayor parte del procesado sea digital.**

4.4 Application Note 048

4.4.1 Signal Conditioning Fundamentals for Computer-Based Measurement Systems

4.4.1.1 Introduction

Computer-based measurement systems are used in a wide variety of applications. In laboratories, in field services and on manufacturing plant floors, these systems act as general-purpose measurement tools well suited for measuring voltage signals. However, many real-world sensors and transducers require signal conditioning before a computer-based measurement system can effectively and accurately acquire the signal. The front-end signal conditioning system can include functions such as signal amplification, attenuation, filtering, electrical isolation, simultaneous sampling, and multiplexing. In addition, many transducers require excitation currents or voltages, bridge completion, linearization, or high amplification for proper and accurate operation. Therefore, most computer-based measurement systems include some form of signal conditioning in addition to plug-in data acquisition DAQ devices, as shown in Figure 1.

This application note introduces the fundamentals of using front-end signal conditioning hardware with computer-based measurement systems. First, the signal conditioning requirements of the most common transducers are discussed. This application note also describes some general signal conditioning functions and briefly discusses the role of signal conditioning products such as the National Instruments Signal Conditioning eXtension for Instrumentation (SCXI) or Signal Conditioning Components (SCC) product lines.

4.4.1.2 Transducers

Transducers are devices that convert one type of physical phenomenon, such as temperature, strain, pressure, or light into another. The most common transducers convert physical quantities to electrical quantities, such as voltage or resistance. Transducer characteristics define many of the signal conditioning requirements of your measurement system. Table 1 summarizes the basic characteristics and conditioning requirements of some common transducers.

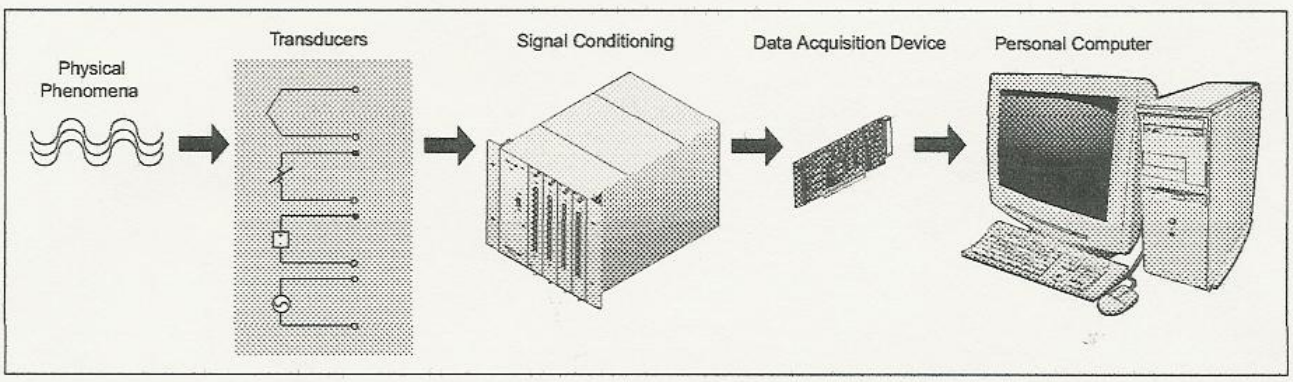


Figure 1. Signal conditioning is an important component of a PC-based DAQ system.

Sensor	Electrical characteristics	Signal conditioning requirement
Thermocouple	Low voltage output Low sensitivity Non linear output	Reference temperature sensor(for cold junction compensation) High amplification Linearization
RTD	Low resistance(100 ohms typical) Low sensitivity Non linear output	Current excitation Four ire/three wire configuration Linearization
Strain gage	Low resistance device Low sensitivity Non linear output	Voltage or current excitation High amplification Bridge completion Linearization Shunt calibration
Current output device	Current loop output (4-20 ma typical)	Precision resistor
Thermistor	Resistive device High resistance and sensitivity Very non linear output	Current or voltage excitation With reference resistor Linearization
Active accelerometers	High level voltage or current output Linear output	Power source Moderate amplification
AC linear variable diferential transformer (LVDT)	AC voltage output	AC excitation Demodulation Linearization

Table 1. Electrical Characteristics and Basic Signal Conditioning Requirements of Common Transducers

4.4.1.3 Thermocouples

The most popular transducer for measuring temperature is the *thermocouple*. The thermocouple is an inexpensive, rugged device that can operate over a very wide range of temperatures. However, the thermocouple has unique signal conditioning requirements. A thermocouple operates on the principle that the junction of two dissimilar metals generates a voltage that varies with temperature. Measuring this voltage is difficult because connecting the thermocouple to the terminals of a DAQ board creates what is called the *reference junction* or *cold junction*, shown in Figure 2. These additional junctions act as thermocouples themselves and produce their own voltages. Thus, the final measured voltage, VMEAS, includes both the thermocouple and cold junction voltages. The method used to compensate for these unwanted cold-junction voltages is called *cold-junction compensation*.

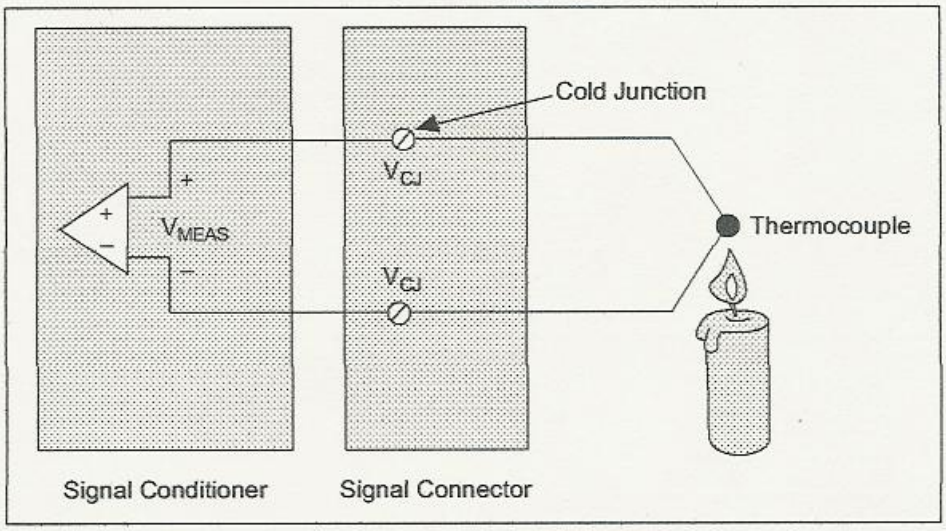


Figure 2. The connection of thermocouple wires to a measurement system creates an additional thermoelectric junction, called the cold junction, which must be compensated for with signal conditioning.

There are two general approaches to cold-junction compensation – hardware and software compensation. Hardware compensation uses a special circuit that applies the appropriate voltage to cancel the cold-junction voltage. Although you need no software for hardware compensation, each thermocouple type must have its own compensation circuit that works at all ambient temperatures. Cold-junction compensation in software, on the other hand, is very flexible and requires only knowing the ambient temperature. If you use an additional sensor to directly measure the ambient temperature at the cold junction, you can compute the appropriate compensation for the unwanted thermoelectric voltages. This approach is why many signal conditioning accessories are equipped with direct-reading temperature sensors, such as thermistors or semiconductor sensors. Software cold-junction compensation follows this process:

1. Measure the temperature of the reference junction and compute the equivalent thermocouple voltage for this
junction using standard thermocouple tables or polynomials.
2. Measure the output voltage (VMEAS) and add – not subtract – the reference-junction voltage computed in Step 1.
3. Convert the resulting voltage to temperature using standard thermocouple polynomials or look-up tables.

Sensitivity is another characteristic to consider with thermocouple measurements. Thermocouple outputs are very low level and change only 7 to 50 µV for every 1 °C change in temperature. You can increase the sensitivity of the system with a low-noise, high-gain amplification of the signal. For example, a plug-in DAQ board with an analog input range of ±5 V, an amplifier gain of 100, and a 12-bit analog-to-digital converter (ADC) has the following resolution:

$$10V/(10^{12} - 100) = 24\ uV/bit$$

The same DAQ board with a signal conditioning amplifier gain of 1000 has a resolution of 2.4 µV/bit, which corresponds to a fraction of a degree Celsius. More importantly, an external signal conditioner can amplify the low-level thermocouple signal near the source to minimize noise corruption. A high-level amplified signal suffers much less corruption from radiated noise in the environment.

4.4.1.4 RTDs

Another popular temperature sensing device is the RTD, which is known for its stability and accuracy over a wide temperature range. An RTD consists of a wire coil or deposited film of pure metal whose resistance increases with temperature. Although different types of RTDs are available the most popular type is made of platinum and has a nominal resistance of 100 W at 0 °C. Because RTDs are passive resistive devices, you must pass a current through the RTD to produce a voltage that a DAQ board can measure. RTDs have relatively low resistance (100 W) that changes only slightly with temperature (less than 0.4 W/°C), so you might need to use special configurations that minimize errors from lead wire resistance.

For example, consider the measurement of a 2-wire RTD in Figure 3. With this RTD, labeled RT, the voltage drops caused by the excitation current, IEXC, passing through the lead resistance, RL, add to the measured voltage, VO.

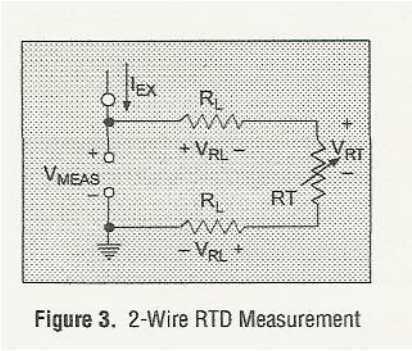


Figure 3. 2-Wire RTD Measurement

For longer lead length, the 4-wire RTD in Figure 4 is a better choice. With a 4-wire RTD, one pair of wires carries the excitation current through the RTD; the other pair senses the voltage across the RTD. Because only negligible current flows through the sensing wires, the lead resistance error is very small.

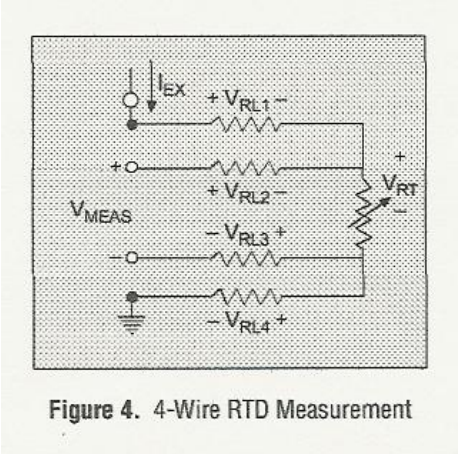


Figure 4. 4-Wire RTD Measurement

To keep costs down, RTDs are also available in 3-wire configurations. The 3-wire RTD is most effective in a Wheatstone bridge configuration (see the following *Strain Gauges* section). In this configuration, the lead resistances are located in opposite arms of the bridge, so their errors cancel each other out.

4.4.1.5 Strain Gauges

The strain gauge is the most common device used in mechanical testing and measurements. The most common type is the bonded resistance strain gauge, which consists of a grid of very fine foil or wire. The electrical resistance of the grid varies linearly with the strain applied to the device. When using a strain gauge, you bond the strain gauge to the device under test, apply force, and measure the strain by detecting changes in resistance. Strain gauges are also used in sensors that detect force or other derived quantities, such as acceleration, pressure, and vibration. These sensors generally contain a pressure sensitive diaphragm with strain gauges mounted to the diaphragm.

Because strain measurement requires detecting relatively small changes in resistance, the Wheatstone bridge circuit is almost always used. The Wheatstone bridge circuit consists of four resistive elements with a voltage excitation supply applied to the ends of the bridge. Strain gauges can occupy one, two or four arms of the bridge, with any remaining positions filled with fixed resistors. Figure 5 shows a configuration with a half-bridge strain gauge consisting of two strain gauge elements, RG1 and RG2, combined with two fixed resistors, R1 and R2.

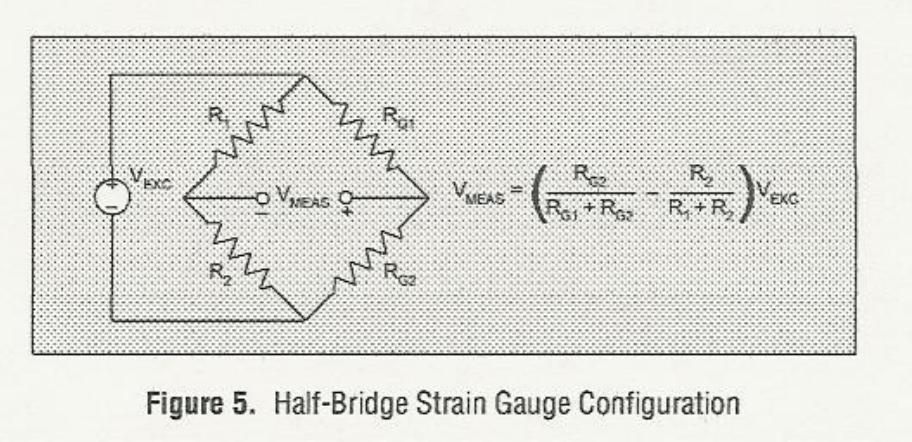


Figure 5. Half-Bridge Strain Gauge Configuration

With a voltage, VEXC, powering the bridge the DAQ system measures the voltage across the bridge:

$$V_0 = [(R_{G2} / (R_{G1} + R_{G2})) - (R_2 / (R_1 + R_2))] V_{EXC}$$

When the ratio of R_{G1} to R_{G2} equals the ratio of R_1 to R_2, the measured voltage V_O is 0 V. This condition is referred to as a balanced bridge. As strain is applied to the gauge, their resistance values change, causing a change in the voltage at VO. Full-bridge and half bridge

strain gauges are designed to maximize sensitivity by arranging the strain gauge elements in opposing directions.
For example, the half-bridge strain gauge in Figure 5 includes an element R_{G1}, which is installed so that its resistance increases with positive strain, and an element R_{G2}, whose resistance decreases with positive strain. The resulting V_O responds with a sensitivity that is twice that of a quarter-bridge configuration. Some signal conditioning products have voltage excitation sources, as well as provisions for bridge-completion resistors. Bridge completion resistors should be very precise and stable. Because strain-gauge bridges are rarely perfectly balanced, some signal conditioning systems also perform nulling. Nulling is a process in which you adjust the resistance ratio of the unstrained bridge to balance the bridge and remove any initial DC offset voltage.
Alternatively, you can measure this initial offset voltage and use this measurement in your conversion routines to compensate for unbalanced initial condition.

4.4.1.6 Accelerometers

An accelerometer is a device commonly used to measure acceleration and vibration. It consists of a known mass attached to a piezoelectric element. As the accelerometer moves, the mass applies force to the element and generates a charge. By reading this charge, you can determine acceleration. Accelerometers are directional, measuring acceleration along only one axis. To monitor acceleration in three dimensions, choose a multiaxis accelerometer. Accelerometers are available in two types, passive and active. Passive accelerometers send out the charge generated by the piezoelectric element. Because the signal is very small, passive accelerometers require a charge amplifier to boost the signal and serve as a very high impedance buffer for your measurement device. Active accelerometers include
internal circuitry to convert the accelerometer charge into a voltage signal, but require a constant current source to drive the circuitry.

4.4.1.7 LVDTs

A linear voltage differential transformer (LVDT) is a device commonly used to measure linear displacement. An LVDT consists of a stationary coil assembly and a movable core (see Figure 6). The coil assembly houses a primary and two secondary windings. The core is a steel rod of high magnetic permeability, and is smaller in diameter than the internal bore of the coil assembly, so you can mount the rod and assure that no contact is made with the coil assembly. Thus the rod can move back and forth without friction or wear.
When an AC excitation voltage is applied to the primary winding, a voltage is induced in each secondary winding through the magnetic core. The position of the core determines how strongly the excitation signal couples to each secondary winding. When the core is in the center, the voltage of each secondary coil is equal and 180 degrees out of phase, resulting in no signal. As the core travels to the left of center, the primary coil is more tightly coupled to the left secondary coil, creating an output signal in phase with the excitation signal. As the core travels to the right of center, the primary coil is more tightly coupled to the right secondary coil, creating an output signal 180 degrees out of phase with the excitation voltage.

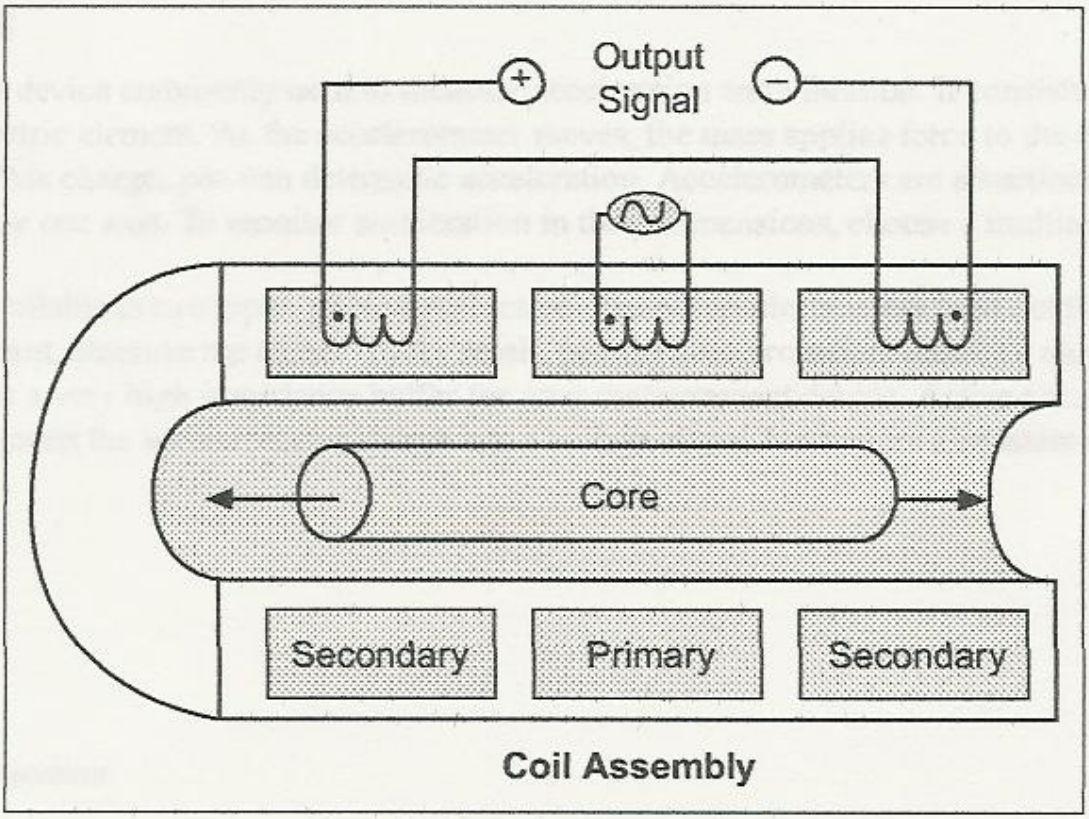


Figure 6. Cross Section of an LVDT

4.4.1.8 Current Signals

Many sensors used in process control and monitoring applications generate a current signal, usually 4 to 20 mA or 0 to 20 mA. Current signals are sometimes used because they are less sensitive to errors such as radiated noise and voltage drops due to lead resistance. Signal conditioning systems must convert this current signal to a voltage signal. To do this easily, pass the current signal through a resistor, as shown in Figure 7.

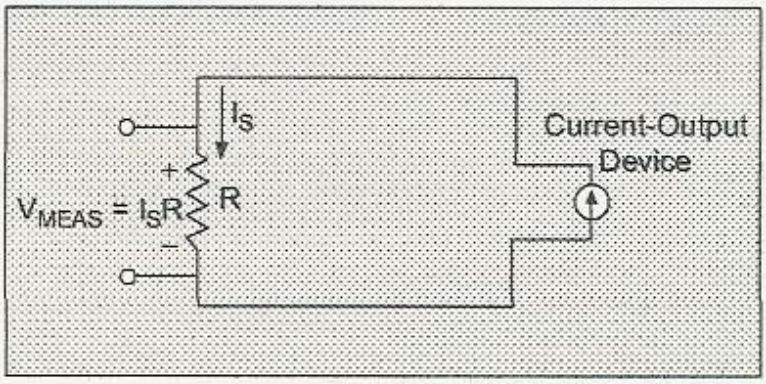


Figure 7. Process current signals, usually 0 to 20 mA or 4 to 20 mA, are converted to voltage signals using precision resistors.

You can then use a DAQ system to measure the voltage VO = ISR that will be generated across the resistor, where IS is the current and R is the resistance. Select a resistor value that has a usable range of voltages, and use a high-precision resistor with a low temperature coefficient. For example, a 249 W, 0.1%, 5 ppm/°C resistor, converts a 4 to 20 mA current signal into a voltage signal that varies from 0.996 to 4.98 V.

4.4.2 General Signal Conditioning Functions

Regardless of the types of sensors or transducers you are using, the proper signal conditioning equipment can improve the quality and performance of your system. Signal conditioning functions are useful for all types of signals, including amplification, filtering, and isolation.

4.4.2.1 Amplification

Because real-world signals are often very small in magnitude, signal conditioning can improve the accuracy of your data. Amplifiers boost the level of the input signal to better match the range of the analog-to-digital converter (ADC), thus increasing the resolution and sensitivity of the measurement. While many DAQ devices include onboard amplifiers for this reason, many transducers, such a thermocouples, require additional amplification.

In addition, using external signal conditioners located closer to the signal source, or transducer, improves the signal-to-noise ratio of the measurement by boosting the signal level before it is affected by environmental noise.

4.4.2.2 Attenuation

Attenuation is the opposite of amplification. It is necessary when the voltages to be digitized are beyond the input range of the digitizer. This form of signal conditioning diminishes the amplitude of the input signal so that the conditioned signal is within range of the ADC. Attenuation is necessary for measuring high voltages.

4.4.2.3 Filtering

Additionally, signal conditioners can include filters to reject unwanted noise within a certain frequency range.

Almost all DAQ applications are subject to some level of 50 or 60 Hz noise picked up from power lines or machinery.

Therefore, most conditioners include lowpass filters designed specifically to provide maximum rejection of 50 to 60 Hz noise.

Another common use of filters is to prevent signal aliasing – a phenomenon that arises when a signal is undersampled (sampled too slowly). The Nyquist theorem states that when you sample an analog signal, any signal components at frequencies greater than one-half the sampling frequency appear in the sampled data as a lower frequency signal. You can avoid this signal distortion only by removing any signal components above one-half the sampling frequency with lowpass filters before the signal is sampled.

4.4.2.4 Isolation

Improper grounding of the system is one of the most common causes for measurement problems, including noise and damaged measurement devices. Signal conditioners with

isolation can prevent most of these problems. Such devices pass the signal from its source to the measurement device without a physical connection by using transformer, optical, or capacitive coupling techniques. Besides breaking ground loops, isolation blocks high-voltage surges and rejects high common-mode voltage and thus protects both the operators and expensive measurement equipment.

4.4.2.5 Multiplexing

Typically, the digitizer is the most expensive part of a data acquisition system. By multiplexing, you can sequentially route a number of signals into a single digitizer, thus achieving a cost-effective way to greatly expand the signal count of your system. Multiplexing is necessary for any high-channel-count application.

4.4.2.6 Simultaneous Sampling

When it is critical to measure two or more signals at the same instant in time, simultaneous sampling is required.
Front-end signal conditioning can provide a much more cost-effective simultaneous sampling solution than purchasing a digitizer for each channel. Typical applications that might require simultaneous sampling include vibration measurements and phase difference measurements.

4.4.2.7 Digital Signal Conditioning

Digital signals can also require signal conditioning peripherals. Typically, you should not connect digital signals used in research and industrial environments directly to a DAQ board without some type of isolation because of the possibility of large voltage spikes or large common voltages. Some signal conditioning modules and boards optically isolate the digital I/O signals to remove these spurious signals. Digital I/O signals can control electromechanical or solid-state relays to switch loads such as solenoids, lights, and motors. You can also use solid-state relays to sense high-voltage field signals and convert them to digital signals.

4.4.3 Signal Conditioning Systems

The signal conditioning functions discussed in this application note are implemented in different types of signal conditioning products. These products cover a very wide range of price and capability.

4.4.3.1 SCXI

SCXI is a front-end signal conditioning and switching system for various measurement devices, including plug-in data acquisition and DMM devices. An SCXI system consists of a rugged chassis that houses shielded signal conditioning modules that amplify, filter, isolate, and multiplex analog signals from thermocouples or other transducers. SCXI is designed for large measurement systems or systems requiring high-speed acquisition.

System features include:
- Modular architecture – choose your measurement technology
- Expandability – expand your system to 3,072 channels

• Integration – combine analog input, analog output, digital I/O, and switching into a single, unified platform
• High bandwidth – acquire signals at an aggregate rate up to 333 kHz
• Connectivity – select from SCXI modules with thermocouple connectors or terminal blocks
For complete information about the SCXI product line, please visit **ni.com/sigcon**

4.4.3.2 SCC

SCC is a front-end signal conditioning system for E Series plug-in data acquisition devices. An SCC system consists of a shielded carrier that holds up to 20 single or dual-channel SCC modules for conditioning thermocouples and other transducers. SCC is designed for small measurement systems where you need only a few channels of each signal type, or for portable applications. SCC systems also offer the most comprehensive and flexible signal connectivity options.
System features include:

- • Modular architecture – select your measurement technology on a per-channel basis
- • Small-channel systems – condition up to 16 analog input and eight digital I/O lines
- • Low-profile/portable – integrates well with other laptop computer measurement technologies
- • High bandwidth – acquire signals at rates up to 1.25 MHz
- • Connectivity – incorporates panelette technology to offer custom connectivity to thermocouple, BNC, LEMO® (B Series), and MIL-Spec connectors

For complete information about the SCC product line, visit **ni.com/sigcon**

4.4.3.3 5B Series

5B is a front-end signal conditioning system for plug-in data acquisition devices. A 5B system consists of eight or 16 single-channel modules that plug into a backplane for conditioning thermocouples and other analog signals. National Instruments offers a complete line of 5B modules, carriers, backplanes, and accessories. For more information, visit **ni.com/sigcon**

4.4.3.4 FieldPoint

FieldPoint is a distributed measurement system for monitoring or controlling signals in light industrial applications. A FieldPoint system includes a serial or Ethernet network module and up to nine I/O modules in a bank. Each I/O module can measure eight or 16 channels. FieldPoint is designed for applications with small clusters of I/O points at several different locations. FieldPoint is also an attractive solution for cost-sensitive applications performing low-speed monitoring.

System features include:

- • Modular architecture – select your measurement technology on a per-module basis
- • Expandability – network multiple banks to a single system
- • Integration – combine analog input, analog output, digital I/O, and switching into a single, unified platform

- • Low-speed monitoring – up to 100 Hz
- • Light-industrial grade – 70 °C temperature range, hot-swappable, programmable start-up states, watchdog timers.

For complete information about the FieldPoint product line, please visit **ni.com/fieldpoint**

4.4.4 Conclusion

Signal conditioning is an important component of any complete measurement system. No matter which sensor you are using, signal conditioning can improve the accuracy, effectiveness, and safety of your measurements because of capabilities such amplifications, isolation, and filtering. National Instruments can supply you with the signal conditioning and instrumentation front-end solution you need for accurate measurements.

4.5 Linealización.(3.1)

4.5.1 What Is Linearization?

Engineers often use linearization in the design and analysis of control systems and physical models. Successful linearization depends on an understanding of important linearization concepts and factors affecting linearization, discussed here.

4.5.1.1 Purpose of Linearization
Simplify system design and analysis using linearized models

4.5.1.2 Understanding Linearization
Factors affecting linearization of Simulink models

4.5.1.3 Understanding Open Loop Analysis
Effects of feedback loops in linearization

Purpose of Linearization
Many common control system analysis and design methodologies require linear, time-invariant models. However, control systems and physical models created with Simulink are often nonlinear and time-varying.
Linearization is the approximation of a nonlinear system as a linear system, based on the assumption that the system is almost linear within a certain range of operation. With a linearized model you can
Use the Control System Toolbox LTI Viewer to display and analyze dynamic behaviors of a model
Tune feedback gains and design compensators for a system
Express a model as a transfer function, state space model, or zero-pole-gain model
Determine the response of a model to arbitrary input signals
A linearized model can provide a good approximation to a nonlinear system when created and used carefully. Factors affecting the accuracy of the approximation addressed in this chapter are

- Choice of operating points. **See Operating Points**.
- Understanding the equations for the linearized model. See **Linearization of Nonlinear Models**.
- Controlling the effect of feedback loops. See **Understanding Open Loop Analysis**.

Understanding Linearization
Understanding the process of linearization with Simulink Control Design depends on first understanding several concepts such as operating points (define the point at which the linearization takes place), the relationship between linearization theory and linearization of Simulink models, and the effects of feedback loops. The remainder of this chapter discusses these concepts in the following sections.

- **Operating Points**
- **Linearization of Nonlinear Models**
- **Linearization of Discrete-Time Models**
- **Linearization of Multi-Rate Models**
- **Linearization of Simulink Models**
- **Understanding Open Loop Analysis**

Subsequent chapters give information on linearization using Simulink Control Design.

Operating Points

The operating point of a dynamic system defines its overall *state* at a given time. For example, in a model of a car engine, variables such as engine speed, throttle angle, engine temperature, and surrounding atmospheric conditions typically describe the operating point. The level of the operating point affects the system's behavior. For example, the behavior of a car engine can vary greatly when it operates at high or low elevations.

A linearized model is an approximation that is valid in a small region around the operating point of the system. Near the operating point the approximation will be good, while far away it will be poor. A linearized model of a car being operated at 3000 ft. will be very accurate at elevations close to 3000 ft. but less accurate as the car travels higher or lower.

The following figure shows a nonlinear function, $y = x^2$, and a linear function, $y = 2x - 1$. The linear function is an approximation to the nonlinear function about the operating point x=1, y=1. Near this operating point, the approximation is good. Away from this operating point, the approximation is poor. The precise boundaries of this region are often somewhat arbitrary. The following figure shows a possible region of good approximation for the linearization of $y = x^2$.

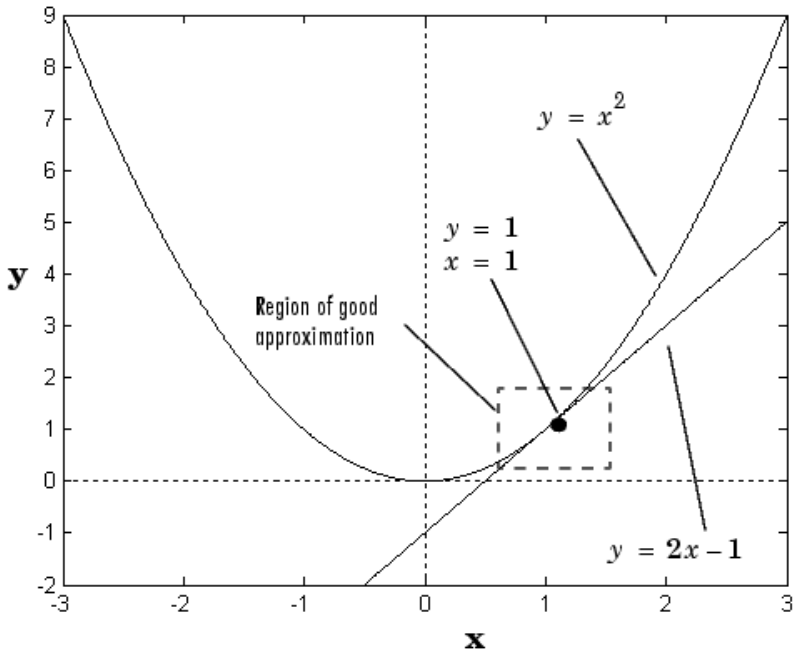


Figure 2-1: Linear Approximation

When creating a linearized model from a Simulink model, the choice of operating point is important as it will determine the accuracy of the approximation. Choose an operating point that is very close to the expected operating values of the system. One way to do this is with an equilibrium operating point, described in the next section.

Equilibrium Operating Points

The equilibrium operating point remains steady and constant with time. It is also known as a **steady state** or trimmed operating point. For example, a car operating on cruise control on a flat road maintains a constant speed. Its operating point is steady, or at equilibrium, although a controller stabilizes the system.

A hanging pendulum provides an example of a stable equilibrium operating point. When the pendulum hangs straight down it's position does not change with time since it is at an equilibrium position. When it's position deviates slightly from this position, it always returns to the equilibrium; small changes in the operating point do not cause the system to leave the region of good approximation around the equilibrium value.

An example of an unstable equilibrium operating point is a pendulum that points upwards. As long as the pendulum points *exactly* upwards, it is steady at this equilibrium state. However, when the pendulum deviates slightly from this state, it swings downwards and the operating point leaves the region around the equilibrium value.

A model linearized about a stable equilibrium operating point is likely to remain within the region around the equilibrium value. This model will give a good approximation to the nonlinear model. A model linearized about an unstable equilibrium operating point is not likely to remain within the region around the equilibrium value. This model gives a poor approximation to the nonlinear model once it deviates from this equilibrium point, unless a controller is designed to stabilize the system. The magnetic ball system in **Linearizing Models** gives an example of an unstable equilibrium that is stabilized by a controller.

Simulink Control Design provides several methods for specifying the operating point of a model. Spec**ifying Operating Points**, and **Specifying Operating Points Using Functions** describe these methods.

Linearization of Nonlinear Models

The following figure shows a block diagram consisting of an external input signal, $u(t)$, a measured output signal, $y(t)$, and a nonlinear system that describes the system's states and its dynamic behavior, P.

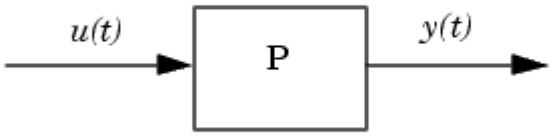


Figure 2-2: Block Diagram

The block diagram is a visual representation of a nonlinear system. You can also express the system in terms of the state space equations

$$\begin{aligned} \dot{x}(t) &= f(x(t), u(t), t) \\ y(t) &= g(x(t), u(t), t) \end{aligned}$$

where $x(t)$ represents the system's states, $u(t)$ represents the inputs, and $y(t)$ represents the outputs. In these equations, the variables vary continuously with time. Discrete-time and multi-rate models are discussed in the section **Linearization of Discrete-Time Models** and **Linearization of Multi-Rate Models**.

A linear time-invariant approximation to this system is valid in a region around the operating point at $t=t_0$, $x(t_0)=x_0$, and $u(t_0)=u_0$. If the values of the system's states, $x(t)$ and inputs, $u(t)$ are close enough to the operating point, the system will behave approximately linearly.

To describe the linearized model, it helps to first define a new set of variables centered about the operating point of the states, inputs, and outputs:

$$\begin{aligned} \delta x(t) &= x(t) - x_0 \\ \delta u(t) &= u(t) - u_0 \\ \delta y(t) &= y(t) - y_0 \end{aligned}$$

The value of the outputs at the operating point is given by $y(t_0)=g(x_0,u_0,t_0)=y_0$.

> **Note** When comparing a linearized model with the original model, remember that the convention used in this book is to write the linearized model in terms of δx, δu, and δy. The value of each of these variables at the operating point is zero.

The linearized state space equations written in terms of $\delta x(t)$, $\delta u(t)$, and $\delta y(t)$ are

$$\begin{aligned} \delta\dot{x}(t) &= A\delta x(t) + B\delta u(t) \\ \delta y(t) &= C\delta x(t) + D\delta u(t) \end{aligned}$$

where A, B, C, and D are constant coefficient matrices. These matrices are defined as the Jacobians of the system, evaluated at the operating point

The transfer function of the linearized model can be used in place of the system, P, in the diagram of **Figure 2-2**. To find the transfer function, divide the Laplace transform of $\delta y(t)$ by the Laplace transform of $\delta u(t)$:

$$A = \left.\frac{\partial f}{\partial x}\right|_{t_0, x_0, u_0} \qquad B = \left.\frac{\partial f}{\partial u}\right|_{t_0, x_0, u_0}$$

$$C = \left.\frac{\partial g}{\partial x}\right|_{t_0, x_0, u_0} \qquad D = \left.\frac{\partial g}{\partial u}\right|_{t_0, x_0, u_0}$$

$$P_{lin}(s) = \frac{\delta Y(s)}{\delta U(s)}$$

Linearization of Discrete-Time Models

Discrete-time models are similar to continuous models, discussed in the previous section, with the exception that the values of system variables change at discrete times, t_k, where k is an integer value. The state-space equations for a nonlinear, discrete-time system are

$$x_{k+1} = f(x_k, u_k, t_k)$$
$$y_k = g(x_k, u_k, t_k)$$

A linear time-invariant approximation to this system is valid in a region around the operating point

$$t_k = t_{k_0}, x_k = x_{k_0}, u_k = u_{k_0}, \text{and } y_k = g(x_{k_0}, u_{k_0}, t_{k_0}) = y_{k_0}$$

If the values of the system's states, x_k, inputs, u_k, and outputs, y_k, are close enough to the operating point, the system will behave approximately linearly. As with continuous time systems it is helpful to define variables centered about the operating point values

$$\delta x_k = x_k - x_{k_0}$$
$$\delta u_k = u_k - u_{k_0}$$
$$\delta y_k = y_k - y_{k_0}$$

where the value of the outputs at the operating point are defined as:

$$y_{k_0} = g(x_{k_0}, u_{k_0}, t_{k_0})$$

The linearized state-space equations can then be written in terms of these new variables

$$\delta x_{k+1} \approx A\delta x_k + B\delta u_k$$
$$\delta y_k \approx C\delta x_k + D\delta u_k$$

where *A*, *B*, *C*, and *D* are given by

$$A = \left.\frac{\partial f}{\partial x_k}\right|_{t_0, x_0, u_0} \qquad B = \left.\frac{\partial f}{\partial u_k}\right|_{t_0, x_0, u_0}$$

$$C = \left.\frac{\partial g}{\partial x_k}\right|_{t_0, x_0, u_0} \qquad D = \left.\frac{\partial g}{\partial u_k}\right|_{t_0, x_0, u_0}$$

Linearization of Multi-Rate Models

Multi-rate models involve states with various sampling rates. This means that the state variables change values at different times and with different frequencies, with some variables possibly changing continuously. The general state-space equations for a nonlinear, multi-rate system are

$$\begin{aligned}
\dot{x}(t) &= f\left(x(t), x_1(k_1), \ldots, x_m(k_m), u(t), t\right) \\
x_1(k_1+1) &= f_1\left(x(t), x_1(k_1), \ldots, x_m(k_m), u(t), t\right) \\
&\vdots \qquad\qquad\qquad\qquad \vdots \\
x_m(k_m+1) &= f_i\left(x(t), x_1(k_1), \ldots, x_m(k_m), u(t), t\right) \\
y(t) &= g\left(x(t), x_1(k_1), \ldots, x_m(k_m), u(t), t\right)
\end{aligned}$$

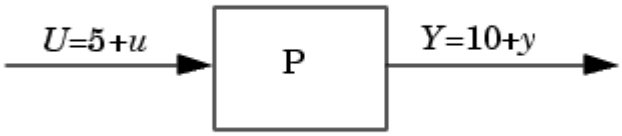
$$t_{k_m} \qquad t_{k_1}$$

where k_1,..., k_m are integer values and ,..., are discrete times. The linearized equations will approximate this system as a single-rate discrete model:

$$\begin{aligned}
\delta x_{k+1} &\approx A\delta x_k + B\delta u_k \\
\delta y_k &\approx C\delta x_k + D\delta u_k
\end{aligned}$$

Linearization of Simulink Models

You apply the linearization concepts when linearizing Simulink models with Simulink Control design. Simulink uses a series of connected *blocks* to model physical systems and control systems. Input and output signals connect the blocks, which represent mathematical operations. The nonlinear system, P, in **Figure 2-2**, now represents a series of connected Simulink blocks.



Simulink linearizes both continuous and discrete-time nonlinear systems by computing the state-space matrices, *A*, *B*, *C*, and *D,* using one of the linearization algorithms described in **Understanding and Controlling Results**. A common method is to perturb the inputs and states by a small amount about their operating point values. The response to these perturbations is measured in the outputs. Both the perturbations and the response are used to compute the matrices. Refer to **Understanding and Controlling Results** for more information.

To linearize models with Simulink Control Design, you must insert linearization input and output points in the model diagram. A linearization input point defines an input to the linearized model while a linearization output point defines an output of the linearized model. Additionally, when the linearized models are computed using numerical perturbation, an input point is the point on the diagram where the small perturbation to the input signal is introduced and an output point is the point on the diagram where the response to this perturbation is measured. **Selecting Linearization Points** gives methods for selecting linearization input and output points with Simulink Control Design.

Understanding Open Loop Analysis

Many control systems contain feedback loops. An example of such a system is shown in this figure.

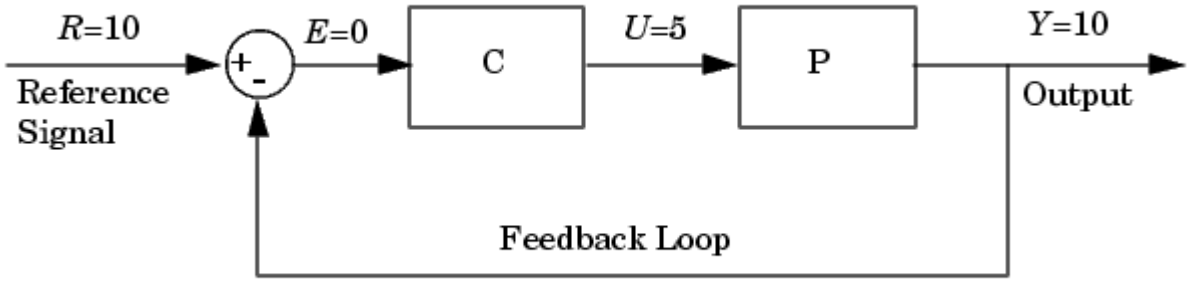


Figure 2-3: Control System with Feedback Loop

The model represented in this figure is at equilibrium. Consider linearizing the plant, P, about this equilibrium operating point by changing the input signal, *U*, by a small amount, *u*, and measuring the change in the output signal, *y*. The portion of the system that you want to linearize is shown in the following figure.

Figure 2-4: Portion of System for Linearization

However, due to the presence of the feedback loop, the change in the output signal will feed back into the controller, C, and then into the plant. This affects the behaviour of the system you are linearizing. In fact, if C and P were linear, the linearized model between *U* and *Y* would be

$$\frac{P(s)}{1+C(s)P(s)}$$

rather than $P(s)$.

You could manually remove the feedback signal from the model in an attempt to resolve this issue. However, as shown in the following figure, this changes the operating point of the system since the error signal, *E*, is now equal to the reference signal, *R*. Linearizing about this new operating point would change the linearization results. Of course, this only makes a difference for non-linear models. When the model is already linear, it has the same form regardless of the operating point.

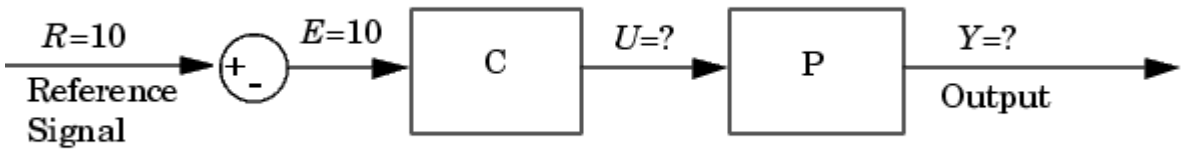


Figure 2-5: Control System with Feedback Signal Removed

When linearizing Simulink models, use Simulink Control Design's capability to label an input or output point as open loop. Doing so ensures that the output signal is not fed back into the model but keeps the operating point the same. In other words, in the linear case, you would compute $P(s)$ rather than $\frac{P(s)}{1+C(s)P(s)}$. **Performing Open Loop Analysis** and **Open Loop Analysis Using Functions** give methods for assigning open loop points in Simulink models using the Simulink Control Design GUI and functions respectively.

4.5.2 Linearizing Models

Use the Simulink Control Design Graphical User Interface (GUI) to linearize Simulink models. With this tool you can insert, inspect, and change input and output points for linearization without adding blocks to the model diagram, perform open loop analysis without manually breaking signal lines, and specify or compute operating points for linearization. Additionally, use the GUI to inspect operating points and results of the linearization (block-by-block), export them to the MATLAB workspace, and display them in the LTI Viewer. You can also save, reload, and compare linearization projects using alternative operating points and parameter values.

4.5.2.1 Overview

An introduction to the linearization process

Overview

The main steps to linearize a model using the Simulink Control Design GUI are

1. Creating or opening a model
2. Opening a linearization project in the Control and Estimation Tools Manager
3. Configuring the model
4. Specifying the operating point
5. Linearizing the model or block
6. Analyzing the results
7. Exporting and saving your work

The following section introduces an example containing a nonlinear system (a levitating magnetic ball). Subsequent sections of this chapter use the example for a detailed discussion of each step.

You can also use the Simulink Control Design command line functions to linearize a model. **Linearizing Models Using Functions** gives detailed information on these functions. For a discussion of the advantages and disadvantages of the GUI versus the command line interface, please refer to **Using the GUI vs. Command Line Functions**.

4.5.2.2 Example: The Magnetic Ball

Derivation of a nonlinear system that illustrates features of Simulink Control Design

Creating or Opening a Simulink Model

Opening the Simulink model of the magnetic ball example

Example: The Magnetic Ball

The electronic circuit in the following figure consists of a voltage source, a resistor, and an inductor in the form of a tightly wound coil. An iron ball beneath the inductor experiences a gravitational force as well as an induced magnetic force (from the inductor) that opposes the gravitational force.

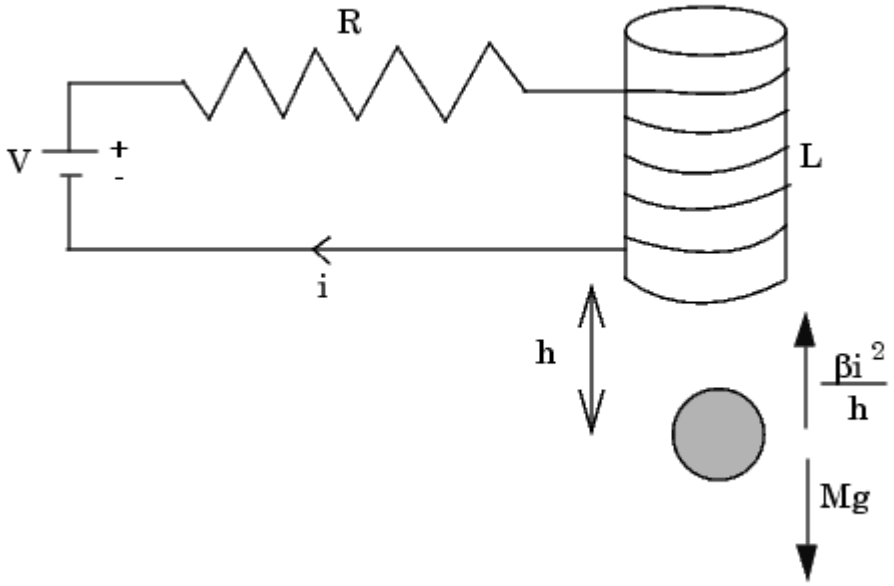


Figure 3-1: Schematic Diagram of Magnetic Ball System

Model Equations

A differential equation for the force balance on the ball is given by

$$M\frac{d^2h}{dt^2} = Mg - \frac{\beta i^2}{h}$$

where *M* is the mass of the ball, *h* is the height (position) of the ball, *g* is the acceleration due to gravity, *i* is the current, and β is a constant related to the magnetic force experienced by the ball. This equation describes the height, *h*, of the ball due to the unbalanced forces acting upon it.

The current in the circuit also varies with time and is given by the following differential equation

$$L\frac{di}{dt} = V - iR$$

where *L* is the inductance of the coil, *V* is the voltage in the circuit, and *R* is the resistance of the circuit.

The system of equations has three states

$$h, \frac{dh}{dt}, i$$

The system also has one input (*V*), and one output (*h*). It is a nonlinear system due to the term in the equation involving the square of *i* and the inverse of *h*. Due to its nonlinearity, you cannot analyze this system using methods for linear-time-invariant (LTI) systems such as step response plots, bode diagrams, and root-locus plots. However, linearizing using Simulink Control Design approximates the nonlinear system as an LTI system. This linearized system can then use the LTI Viewer for display and analysis. Refer to **Purpose of Linearization** for a discussion of the uses of linearized models and **Linearization of Nonlinear Models** for a discussion of the linearization process.

4.6 Filtrado.(3.2)

4.6.1 1.1 Analogue RCL Filter Types

In the following paragraphs, the analogue RCL filter network will be analysed for the four basic filter types: low pass, high pass, band pass, and band stop. Analyzing analogue filter types shows that designing digital IIR filters is, in many cases, much simpler than designing analogue filters.

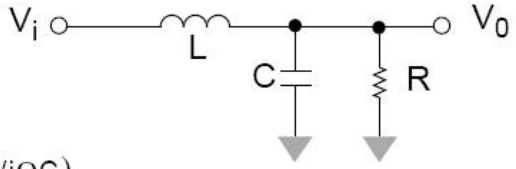
In this analysis, as in all of the following cases, the input is assumed to be a steady-state signal containing a linear combination of sinusoidal components whose rms (or peak) amplitudes are constant in time. This assumption allows simple analytic techniques to be used in determining the network response. Even though these results will then be applied to real-world signals that may not satisfy the original steady-state assumption, the deviation of the actual response from the predicted response is small enough to neglect in most cases.
General analysis techniques consist of a linear combination of steady-state and transient response solutions to the differential equations describing the network.

4.6.2 1.2 Analogue Low pass Filter

The passive RCL circuit forming a low pass filter network is shown in Figure 1-1 where the transfer function, H(s), is derived from a voltage divider analysis of the RCL network. This approach is valid since the effect of C and L can be described as a complex impedance (or reactance, X_C and X_L) under steady state conditions; s is a complex variable of the complex transfer function, H(s). The filter frequency response is found by evaluating H(s) with $s = J\Omega$, where $\Omega = 2 p f$ and f is the frequency of a sinusoidal component of the input signal. The output signal is calculated from the product of the input signal and $H(j \Omega)$. To facilitate analysis, the input and output signal components are described by the complex value, $e^{j \Omega t} = \cos \Omega t + j \sin \Omega t$. The actual physical input and output signal components are found by taking the real part of this value.
The input is $R\{e^{j \Omega t}\} = \cos \Omega t$; the output is $R\{H(j \Omega)e^{j \Omega t}\} = G(\Omega) \cos [\Omega t + f (\Omega)]$.

The previous technique is based upon the solution of the differential equations describing the network when the input is steady state.
Describing the circuit response by H(s) instead of solving the differential equation is a common simplification used in this type of analysis.

$$\frac{V_0}{V_i} = \frac{X_C \| R}{X_L \| R}$$



$$X_c = 1/j\Omega C$$

$$= \frac{(R/j\Omega C)/(R + 1/j\Omega C)}{j\Omega L + (R/j\Omega C)/(R + 1/j\Omega C)}$$

$$X_L = j\Omega L$$

$$= \frac{1/LC}{-\Omega^2 + j\Omega/RC + 1/LC}$$

$$\Omega_c = \frac{1}{\sqrt{LC}}$$

$$= \frac{\Omega_c^2}{-\Omega^2 + jd\Omega_c\Omega + \Omega_c^2}$$

$$d = \sqrt{\frac{L}{R^2 C}}$$

Let s = jΩ and define H(s) = Vo/Vi; then,

$$H(s) = \frac{1}{(s/\Omega_c)^2 + d(s/\Omega_c) + 1}$$

which is the s-domain transfer function. The gain, G(Ω), of the filter is:

$$G(\Omega) \equiv \sqrt{H(s)H^*(s)}\Big|_{s = j\omega}$$

$$= \frac{1}{\sqrt{(1 - \Omega^2/\Omega_c^2)^2 + (d\Omega/\Omega_c)^2}}$$

where * denotes complex conjugate.
The phase angle, ΦΩ, is the angle between the imaginary and real components of H(s).

$$\phi(\Omega) \equiv \tan^{-1}[I\{H(s)\}/R\{H(s)\}]$$

$$= -\tan^{-1}\left[\frac{d(\Omega/\Omega_c)}{1 - (\Omega/\Omega_c)^2}\right] \quad \text{for } \Omega \le \Omega_c$$

$$= -\pi - \tan^{-1}\left[\frac{d(\Omega/\Omega_c)}{1 - (\Omega/\Omega_c)^2}\right] \quad \text{for } \Omega > \Omega_c$$

Figure 1-1 s-Domain Analysis of Second-Order Lowpass Analog Filter

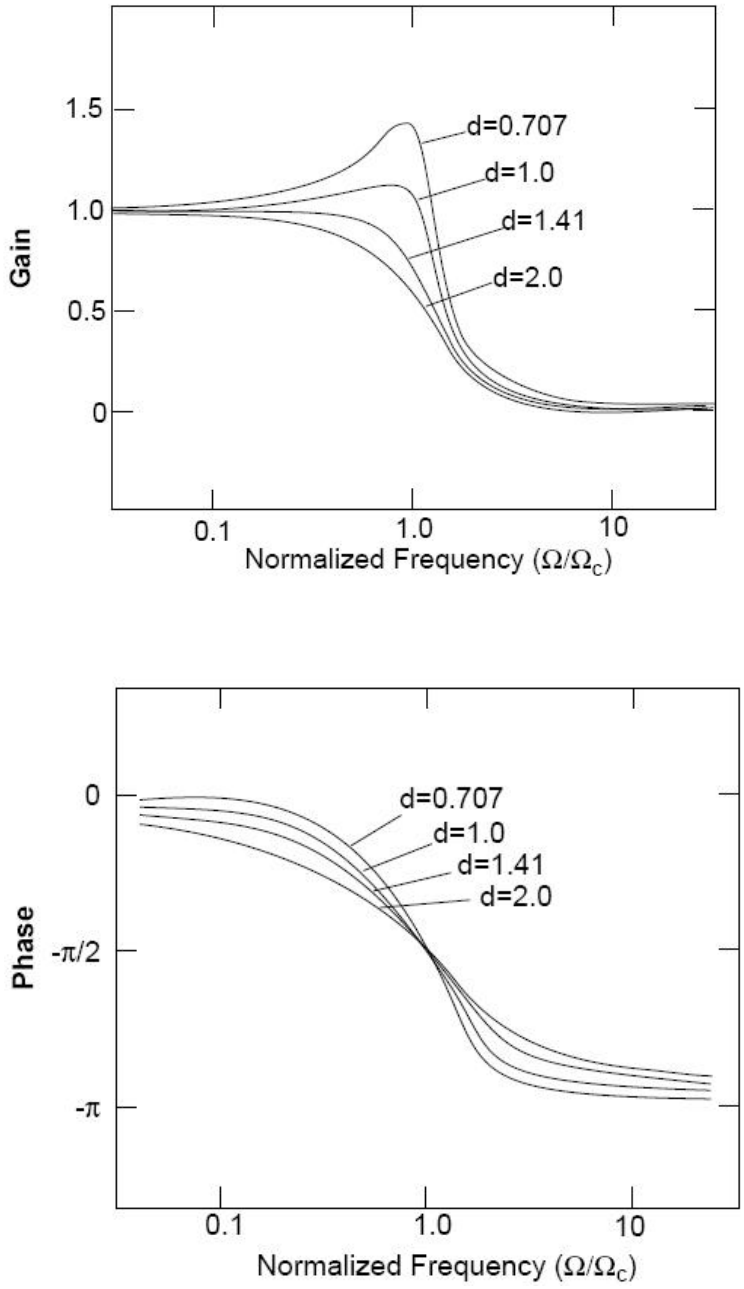


Figure 1-2 Gain and Phase Response of Second-Order Lowpass Analog Filter at Various Values of Damping Factor, d

The magnitude of H(s) is defined as the gain, G(Ω), of the system; whereas, the ratio of the imaginary part to real part of H(s), I{H(jΩ)}/R{H(jΩ)}, is the tangent of the phase, f(Ω), introduced by the filter. If the input signal is A_K sin ($\Omega_K t + f_K$), then the output signal is $A_K G(\Omega_K)$ sin [$\Omega_K t + f_K + f(\Omega_K)$] Figure 1-2 shows the gain, G(W), and phase, f(Ω), plots for the second-order low pass network of Figure 1-1 for various values of damping factor, d; d also controls the amplitude and position of the peak of the normalized response curve.

The frequency corresponding to the peak amplitude can be easily found by taking the derivative of G(Ω) (from the equation for G(Ω) in Figure 1-1) with respect to Ω and setting it equal to zero. Solving the resultant equation for Ω then defines Ω_M as the frequency where the peak amplitude occurs. The peak amplitude is then $G_M = G(\Omega_M)$: for $d < \sqrt{2}$. For $d > \sqrt{2}$, $\Omega_M = 0$ is the position of the peak amplitude where $G_M = 1$. When $d = \sqrt{2}$, $G_M = 1$, which gives the maximally flat response curve used in the Butterworth filter design (usually applies only to a set of cascaded sections). Note that Ω_C for a low pass filter is that frequency where the gain is $G(\Omega_C) = 1/d$ and the phase is $f(\Omega_C) = -p/2$.

$$\Omega_M = \Omega_c\sqrt{(1 - d^2/2)} \qquad \text{Eqn. 1-1}$$

$$G_M = \frac{1}{d\sqrt{(1 - d^2/4)}} \qquad \text{Eqn. 1-2}$$

4.6.3 1.3 Analogue High pass Filter

The passive RCL circuit forming a high pass filter network is shown in Figure 1-3 where the transfer function, H(s), is again derived from a voltage divider analysis of the RCL network. The gain and phase response are plotted in Figure 1-4 for different values of damping coefficient. As evidenced, the high pass filter response is the mirror image of the low pass filter response.

4.6.4 1.4 Analogue Band stop Filter

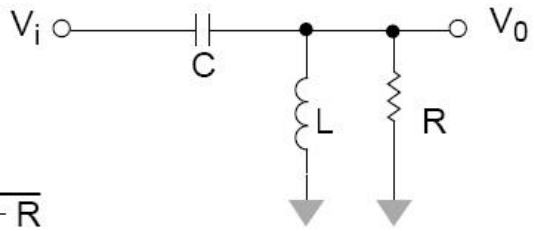
The analogue RCL network for a band stop filter network is simply the sum of the low pass and high pass transfer functions shown in Figure 1-5 where the transfer function, H(s), is again derived from a voltage divider analysis of the RCL network. The gain and phase response are plotted in Figure 1-6 for different values of quality factor, Q, (where Q = 1/d).
Neglecting the departure of real RCL components' values from the ideal case, the attenuation at the center frequency, f_0, is infinite. Also, note that the phase undergoes a 180-degree shift when passing through the center frequency (zero in the s-plane).
Q for band pass and band stop filters is a measure of the width, ΔΩ, of the stopband with respect to the center frequency, Ω_0, i.e., $\Delta\Omega = Q^{-1}\Omega_0$. ΔΩ is measured at the points where $G(\Omega) = 1/\sqrt{2}$.

$$\frac{V_0}{V_i} = \frac{X_L \| R}{X_C + X_L \| R}$$

$$= \frac{j\Omega LR/(j\Omega L + R)}{1/j\Omega C + j\Omega LR/j\Omega L + R}$$

$$= \frac{-\Omega^2}{-\Omega^2 + j\Omega/RC + 1/LC}$$

$$= \frac{-\Omega^2}{-\Omega^2 + jd\Omega_c\Omega + \Omega_c^2}$$



$X_c = 1/j\Omega C$

$X_L = j\Omega L$

$\Omega_c = \frac{1}{\sqrt{LC}}$

$d = \sqrt{\frac{L}{R^2C}}$

Let s = jΩ and define H(s) = Vo/Vi; then,

$$H(s) = \frac{(s/\Omega_c)^2}{(s/\Omega_c)^2 + d(s/\Omega_c) + 1}$$

which is the s-domain transfer function. The gain, G(Ω), of the filter is:

$$G(\Omega) \equiv \sqrt{H(s)H^*(s)}\Big|_{s = j\omega} = \frac{(\Omega/\Omega_c)^2}{\sqrt{(1 - \Omega^2/\Omega_c^2)^2 + (d\Omega/\Omega_c)^2}}$$

where * denotes complex conjugate.
The phase angle, ΦΩ, is the angle between the imaginary and real components of H(s).

$$\phi(\Omega) \equiv \tan^{-1}[I\{H(s)\}/R\{H(s)\}]$$

$$= \pi - \tan^{-1}\left[\frac{d(\Omega/\Omega_c)}{1 - (\Omega/\Omega_c)^2}\right] \quad \text{for } \Omega \le \Omega_c$$

$$= -\tan^{-1}\left[\frac{d(\Omega/\Omega_c)}{1 - (\Omega/\Omega_c)^2}\right] \quad \text{for } \Omega > \Omega_c$$

Figure 1-3 s-Domain Analysis of Second-Order High pass Analogue Filter

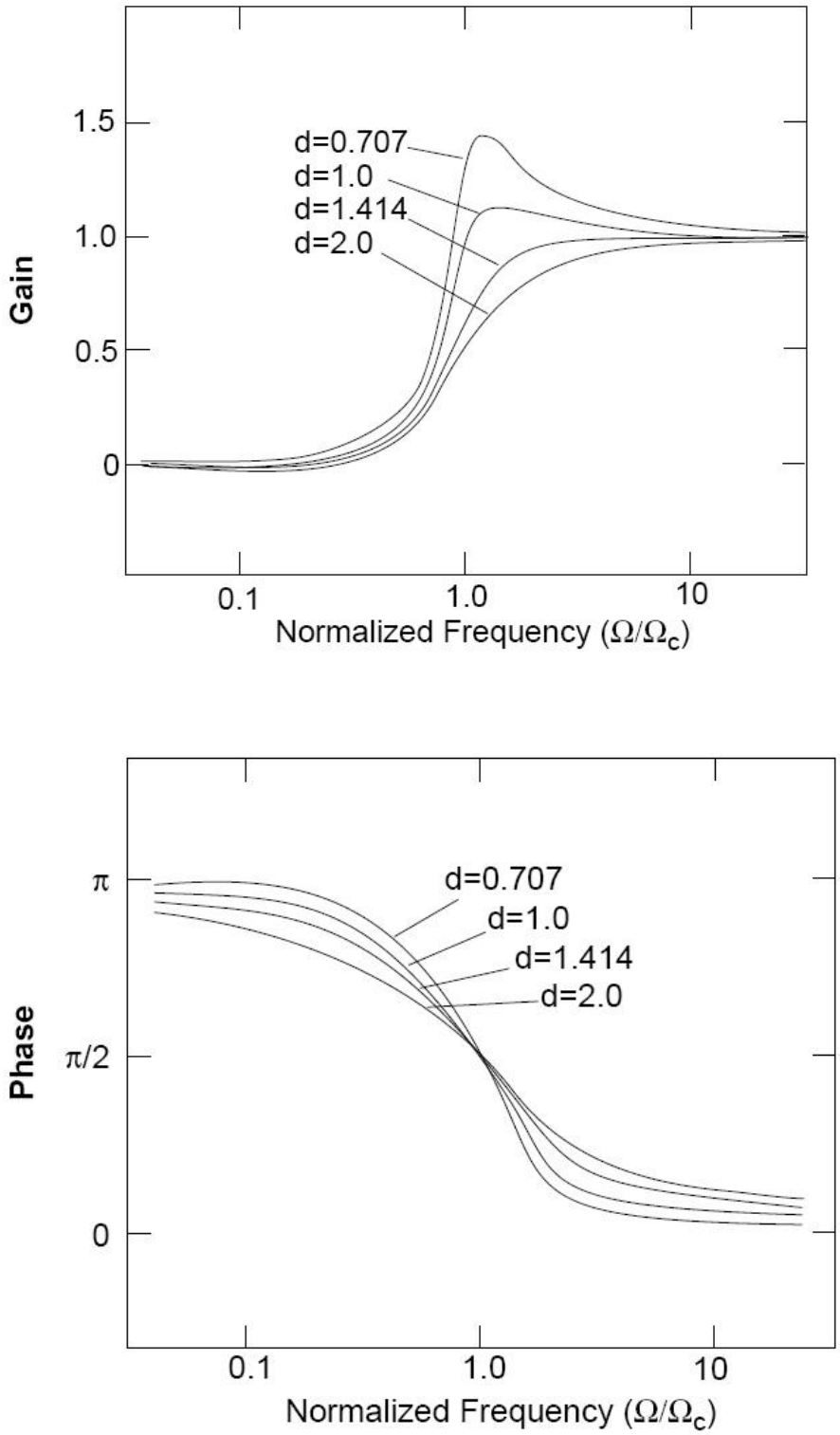


Figure 1-4 Gain and Phase Response of Second-Order High pass Analogue Filter at Various Values of Damping Factor, d

4.6.5 1.5 Analogue Band pass Filter

The passive RCL circuit forming a band pass filter network is shown in Figure 1-7 where the transfer function, H(s), is again derived from a voltage divider analysis of the RCL network. The gain and phase response are plotted in Figure 1-8 for different values of Q. The low pass gain approaches an asymptotic function of $G = (f_C/f)^2$ for $f/f_0 >> 1$. The high pass asymptotic gain is $G = (f_C/f)^2$ for $f/f_C << 1$; whereas, the band stop case approaches unity at zero and infinity with a true zero at the center frequency.
The band pass gain, on the other hand, approaches $G = Q^{-1}f/f_C$ for $f/fc << 1$ and $G = Q^{-1}fc/f$ for $f/fc >> 1$. The primary differences to note in the band pass response are:

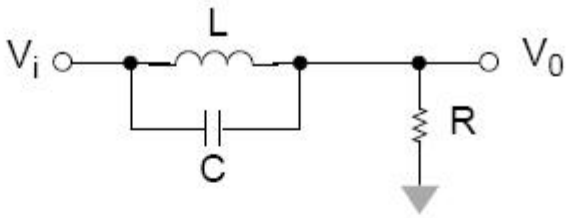
1. the stop band attenuation is 6 dB/octave or 20 dB/decade (since it goes as 1/f); whereas, the low pass and high pass go as l/f^2 (12 dB/ octave, 40 dB/decade)

2. the stop band attenuation asymptote is dependent on the quality factor; whereas, for the low pass and high pass cases, the stop band attenuation asymptote is independent of damping factor, d

3. the maximum value of gain is unity regardless of the filter Q.

The specific features characterizing the band pass, low pass, high pass, and band stop analogue networks are found to be nearly identical in the digital IIR filter equivalents when the sampling frequency is very high as compared to the frequencies of interest. For this reason, it is important to understand the basic properties of the four filter types before proceeding to the digital domain.

$$\frac{V_0}{V_i} = \frac{R}{x_C \| X_L + R}$$



$$X_c = 1/j\Omega C$$

$$= \frac{R}{R + (j\Omega L/j\Omega C)/(j\Omega L + 1/j\Omega C)}$$

$$X_L = j\Omega L$$

$$= \frac{-\Omega^2 + 1/LC}{-\Omega^2 + j\Omega/RC + 1/LC}$$

$$\Omega_c = \frac{1}{\sqrt{LC}}$$

$$= \frac{-\Omega^2 + \Omega_0^2}{-\Omega^2 + j\Omega_0\Omega/Q + \Omega_0^2}$$

$$Q = 1/d = \sqrt{R^2C/L}$$

Let s = jΩ and define H(s) = Vo/Vi; then,

$$H(s) = \frac{(s/\Omega_0)^2 + 1}{(s/\Omega_0)^2 + s/\Omega_0 Q + 1}$$

which is the s-domain transfer function. The gain, G(Ω), of the filter is:

$$G(\Omega) \equiv \sqrt{H(s)H^*(s)}\Big|_{s = j\omega}$$

$$= \frac{\left|1 - (\Omega/\Omega_0)^2\right|}{\sqrt{(1 - \Omega^2/\Omega_0^2)^2 + \Omega/\Omega_0 Q)^2}}$$

where * denotes complex conjugate.

The phase angle, ΦΩ, is the angle between the imaginary and real components of H(s).

$$\phi(\Omega) \equiv \tan^{-1}[I\{H(s)\}/R\{H(s)\}]$$

$$= -\tan^{-1}\left[\frac{(\Omega/\Omega_0 Q)}{1 - (\Omega/\Omega_0)^2}\right]$$

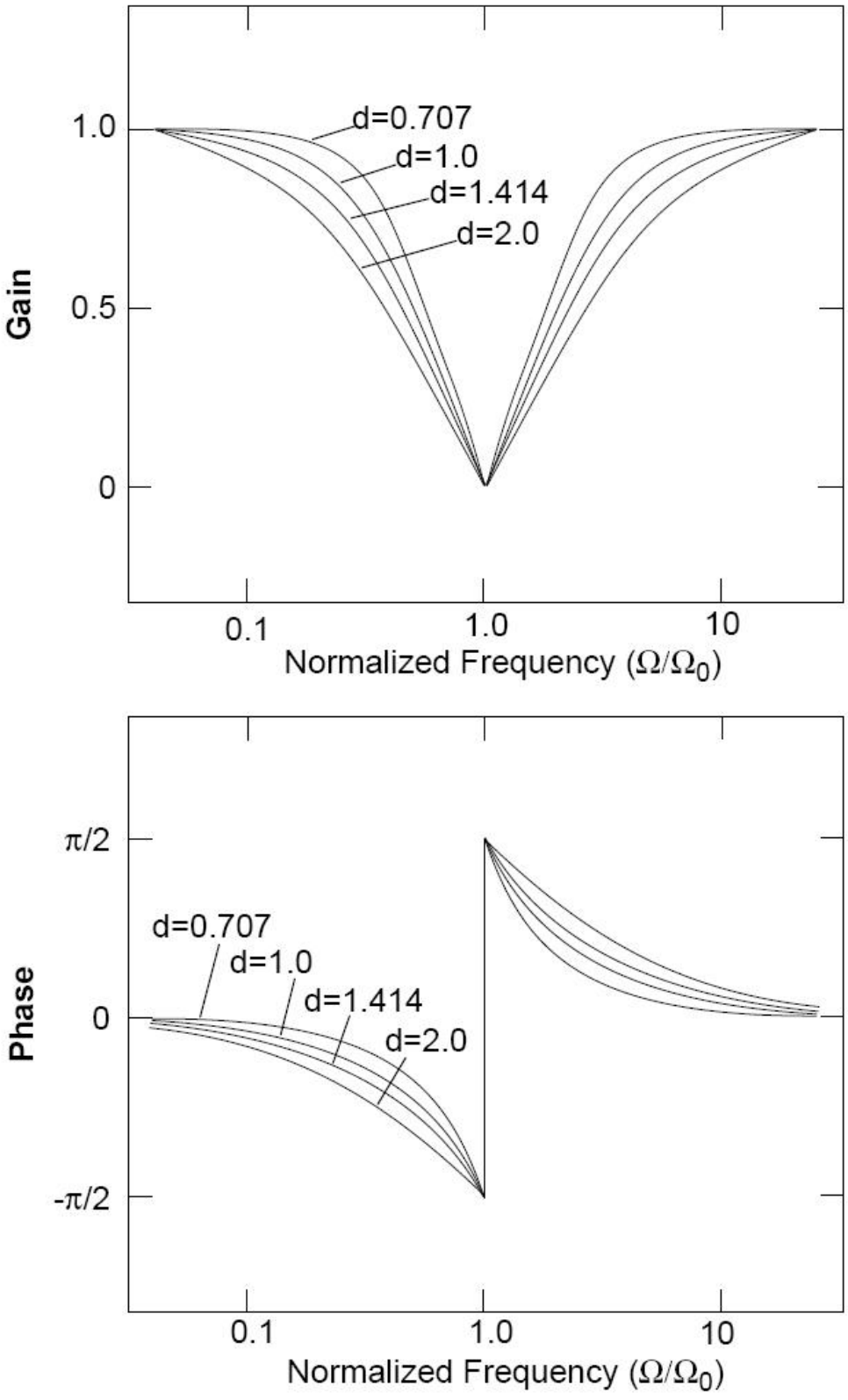
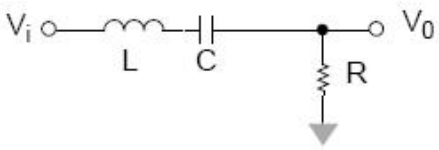


Figure 1-6 Gain and Phase Response of Second-Order Bandstop Analog Filter at Various Values of Damping Factor, d

$$\frac{V_0}{V_i} = \frac{R}{X_L + X_C + R}$$



$$X_c = 1/j\Omega C$$

$$X_L = j\Omega L$$

$$= \frac{R}{j\Omega L + 1/j\Omega + R}$$

$$= \frac{j\Omega R/L}{-\Omega^2 + j\Omega R/L + 1/LC}$$

$$\Omega_c = \frac{1}{\sqrt{LC}}$$

$$= \frac{j\Omega_0 \Omega/Q}{-\Omega^2 + j\Omega_0 \Omega/Q + \Omega_0^2}$$

$$Q = 1/d = \sqrt{R^2 C/L}$$

Let $s = j\Omega$ and define $H(s) = V_o/V_i$; then,

$$H(s) = \frac{s/\Omega_0 Q}{(s/\Omega_0)^2 + s/\Omega_0 Q + 1}$$

which is the s-domain transfer function. The gain, $G(\Omega)$, of the filter is:

$$G(\Omega) \equiv \sqrt{H(s)H^*(s)}\Big|_{s = j\omega}$$

$$= \frac{\Omega/\Omega_0 Q}{\sqrt{(1 - \Omega^2/\Omega_0^2)^2 + (\Omega/\Omega_0 Q)^2}}$$

where $*$ denotes complex conjugate.

The phase angle, $\phi\Omega$, is the angle between the imaginary and real components of H(s).

$$\phi(\Omega) \equiv \tan^{-1}[I\{H(s)\}/R\{H(s)\}]$$

$$= \tan^{-1}\left[\frac{\Omega/\Omega_0 Q}{1 - (\Omega/\Omega_0)^2}\right]$$

Figure 1-7 *s-Domain Analysis of Second-Order Bandpass Analog Filter*

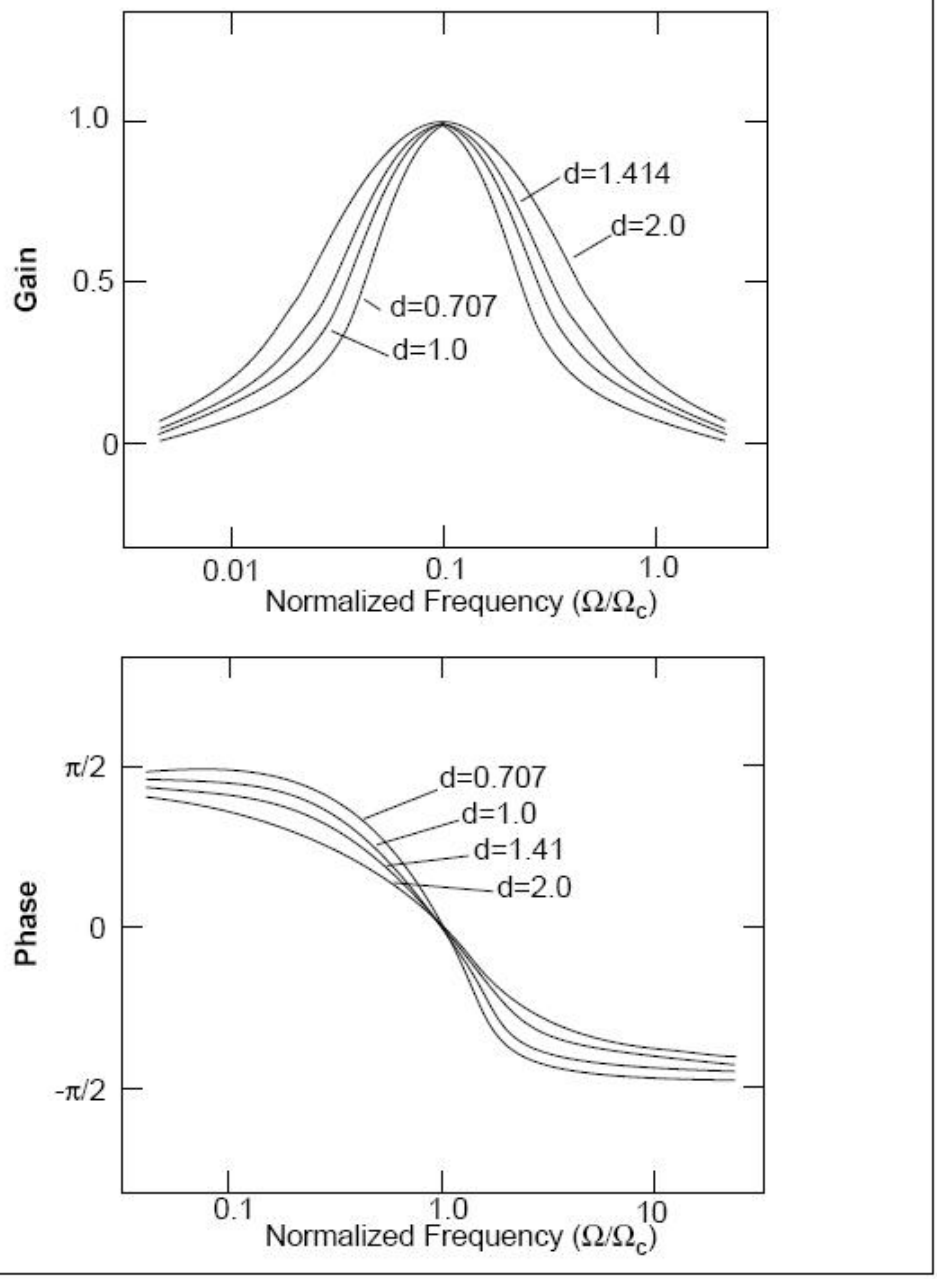


Figure 1-8 *Gain and Phase Response of Second-Order Bandpass Analog Filter at Various Values of Damping Factor, d*

4.7 Escalamiento; tiempo, (3.3)

4.7.1 Scaling From Wikipedia, the free encyclopaedia.

The term **scaling** can have several meanings:

Scaling can be defined as the determination of the interdependency of variables in a physical system. It involves a combination of **dimensional analysis** and **physical reasoning**, and typically requires a good deal of **physical intuition**. It can, however, be used to great advantage in solving otherwise intractable problems. See also nondimensionalization.

In geometry, **scaling** can refer to linear transformations.
Scaling is the process of removing scale(s), as from fish, teeth, or metal.
Scaling is the process of measuring distances on a map.
Scaling is a synonym for climbing.
In computer graphics, **scaling** refers to altering the size of a sprite to make the sprite appear nearer or farther from the player's point of view.
Scaling (computer network) is a relationship in computer networking between a network's ability to continue to function with limited or no degradation in performance as the # of people on the network increases.

4.8 Multiplicación..(3.4)

5 UNIDAD 4. Aplicaciones y Proyectos.

5.1 Aplicaciones.(4.1)

Following you will find a series of applications information from different sources, all concerned with the subjects issued on this course, considering oscillators, PLL, PWM, commutated power sources, and signal conditioning. There is a lot of references from well known semiconductors manufacturers, as well as known standards in industry, communication, and consumer sectors.

5.2 Analogue Micro controllers from Analogue Devices.

Description
Analog Devices' **MicroConverter**® family of precision analogue micro controllers combine precision analogue functions, such as high resolution ADCs and DACs, a voltage reference, and temperature sensor, with an industry-standard micro controller and embedded flash memory.
The ADuC7000 series of products feature an ARM7® 32-bit RISC MCU while the ADuC800 series features an industry standard 8052 MCU core.

5.3 Isolated 0-10V to 4-20 mA Converter Application

By: Clare, Inc.

Industrial controllers and data acquisition equipment frequently require an isolated voltage-to-current loop converter in environments where high common mode noise exist and protection of equipment and personnel from high voltages are required. The **current loop**, usually **4-20 mA**, is used to drive control valves or the input to chart recorders for temperature/pressure monitoring over time for example. Figure 1 shows a simplified block diagram of an isolated pressure transmitter.

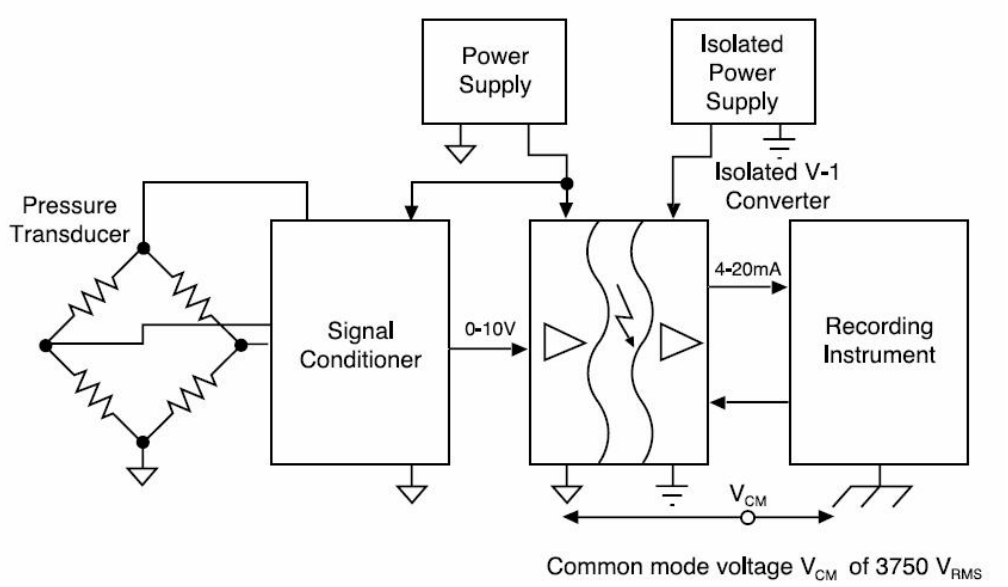


Figure 1. Isolated Pressure Transmitter

The **LIA100P**, with a typical Common Mode Rejection Ratio of 130dB (see figure 1A) and isolation voltage up to 3750VRMS is a good choice for this kind of application.

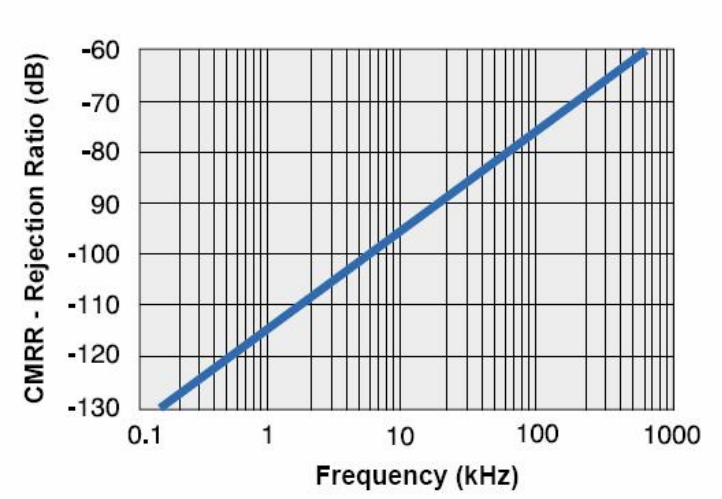


Figure 1A. Common Mode Rejection

The example circuit for this application is shown in figure 1B.

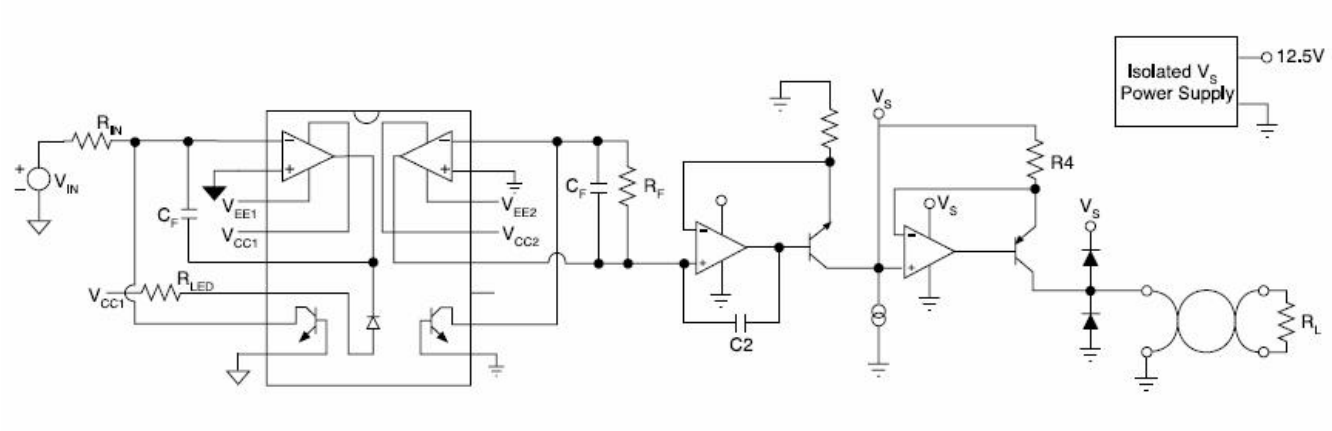


Figure 1B. 0-10V to 4-20mA Converter

The **LIA110P** is in the photovoltaic mode which has linearity comparable to a 13-14 bit D/A converter with 1 LSB non linearity or 0.01% of full scale. The result is a clean, linear conversion from 0-10V to 4-20mA as shown in figure 2.

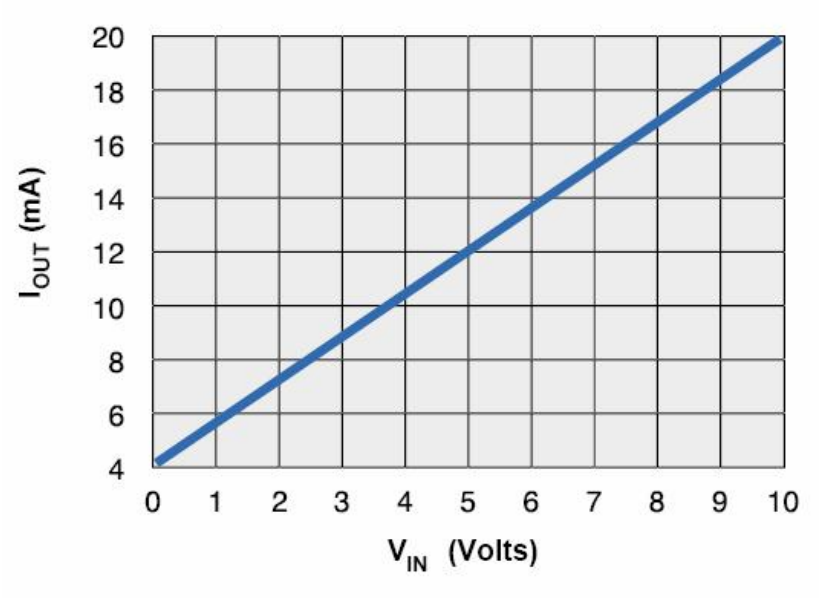


Figure 2.1 OUT(mA) vs. V IN(Volts)

5.4 PWM Motor Speed Controller / DC Light Dimmer

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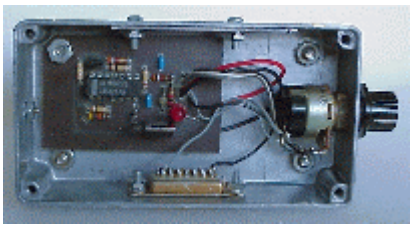

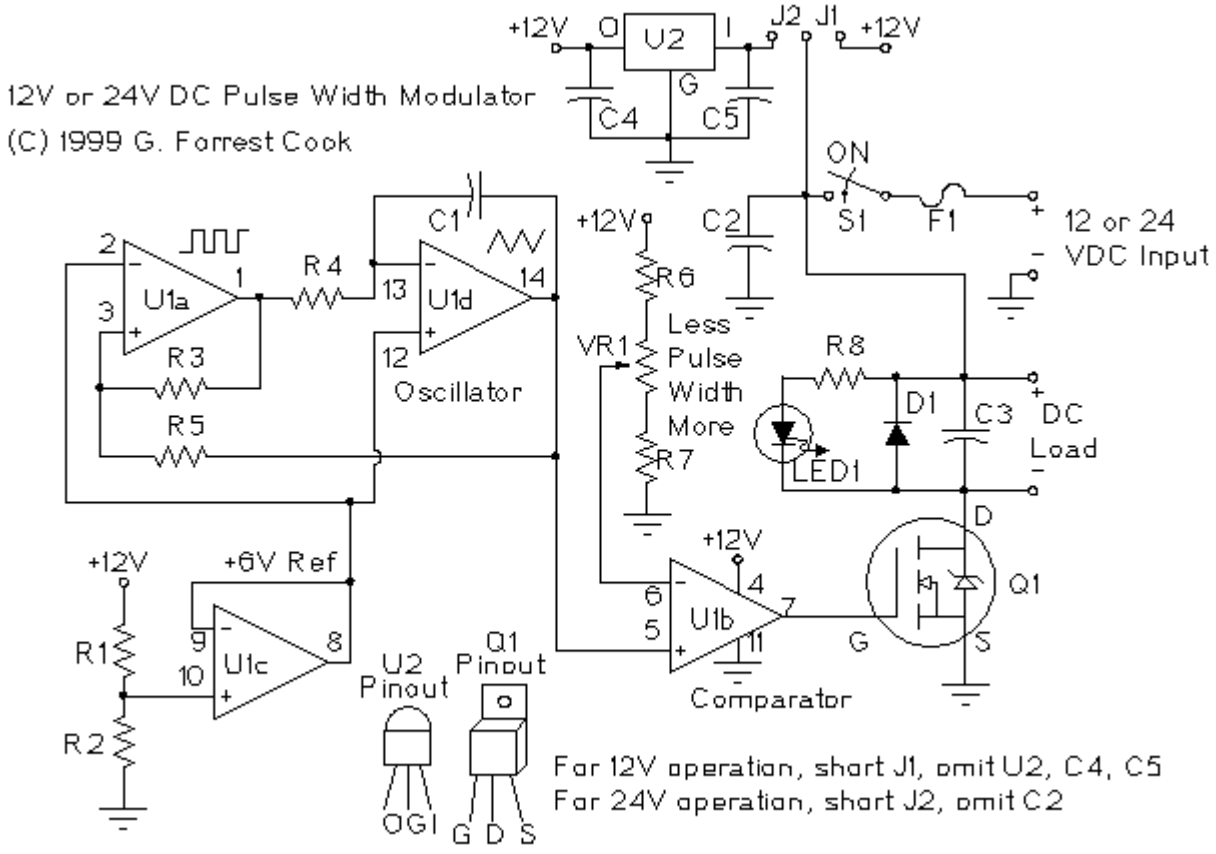

5.5 Pulse Width Modulator for 12 and 24 Volt applications

This circuit was featured in an article in Home Power Magazine #75
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5.5.1 Introduction

A pulse width modulator (**PWM**) is a device that may be used as an efficient light dimmer or DC motor speed controller. The circuit described here is a general purpose device that can control DC devices which draw up to a few amps of current. The circuit may be used in 12 Volt and 24 Volt systems with a few minor changes. This device has been used to control the brightness of an automotive tail lamp and as a motor speed control for small DC fans of the type used in computer power supplies.

A PWM circuit works by making a square wave with a variable on-to-off ratio, the average on time may be varied from 0 to 100 percent. In this manner, a variable amount of power is transferred to the load. The main advantage of a PWM circuit over a resistive power controller is the efficiency, at a 50% level, the PWM will use about 50% of full power, almost all of which is transferred to the load, a resistive controller at 50% load power would consume about 71% of full power, 50% of the power goes to the load and the other 21% is wasted heating the dropping resistor. Load efficiency is almost always a critical factor in alternative energy systems.

One additional advantage of pulse width modulation is that the pulses reach the full supply voltage and will produce more torque in a motor by being able to overcome the internal motor resistances more easily. Finally, in a PWM circuit, common small potentiometers may be used to control a wide variety of loads whereas large and expensive high power variable resistors are needed for resistive controllers.

The main Disadvantages of **PWM** circuits are the added complexity and the possibility of generating radio frequency interference (**RFI**). **RFI** may be minimized by locating the controller near the load, using short leads, and in some cases, using additional filtering on the power supply leads. This circuit has some **RFI** bypassing and produced minimal interference with an **AM** radio that was located under a foot away. If additional filtering is needed, a car radio line choke may be placed in series with the DC power input, be sure not to exceed the current rating of the choke. The majority of the **RFI** will follow the high current path involving the power source, the load, and the switching FET, Q1.

5.5.2 Specifications

PWM Frequency: 400 Hz
Current Rating: 3 A with an **IRF521 FET**, >10A with an **IRFZ34N FET** and heat sink
PWM circuit current: 1.5 ma @ 12V with no LED and no load
Operating Voltage: 12V or 24V depending on the configuration

5.5.3 Theory

The PWM circuit requires a steadily running oscillator to operate. U1a and U1d form a square/triangle waveform generator with a frequency of around 400 Hz.

U1c is used to generate a 6 Volt reference current which is used as a virtual ground for the oscillator, this is necessary to allow the oscillator to run off of a single supply instead of a +/- voltage dual supply.

U1b is wired in a comparator configuration and is the part of the circuit that generates the variable pulse width. U1 pin 6 receives a variable voltage from the R6, VR1, R7 voltage

ladder. This is compared to the triangle waveform from U1-14. When the waveform is above the pin 6 voltage, **U1** produces a high output. Conversely, when the waveform is below the pin 6 voltage, U1 produces a low output. By varying the pin 6 voltage, the on/off points are moved up and down the triangle wave, producing a variable pulse width. Resistors R6 and R7 are used to set the end points of the VR1 control, the values shown allow the control to have a full on and a full off setting within the travel of the potentiometer. These part values may be varied to change the behavior of the potentiometer.

Finally, Q1 is the power switch, it receives the modulated pulse width voltage on the gate terminal and switches the load current on and off through the Source-Drain current path. When Q1 is on, it provides a ground path for the load, when Q1 is off, the load's ground is floating. Care should be taken to insure that the load terminals are not grounded or a short will occur.

The load will have the supply voltage on the positive side at all times. LED1 gives a variable brightness response to the pulse width. Capacitor C3 smooth out the switching waveform and removes some **RFI**, Diode D1 is a flywheel diode that shorts out the reverse voltage kick from inductive motor loads.

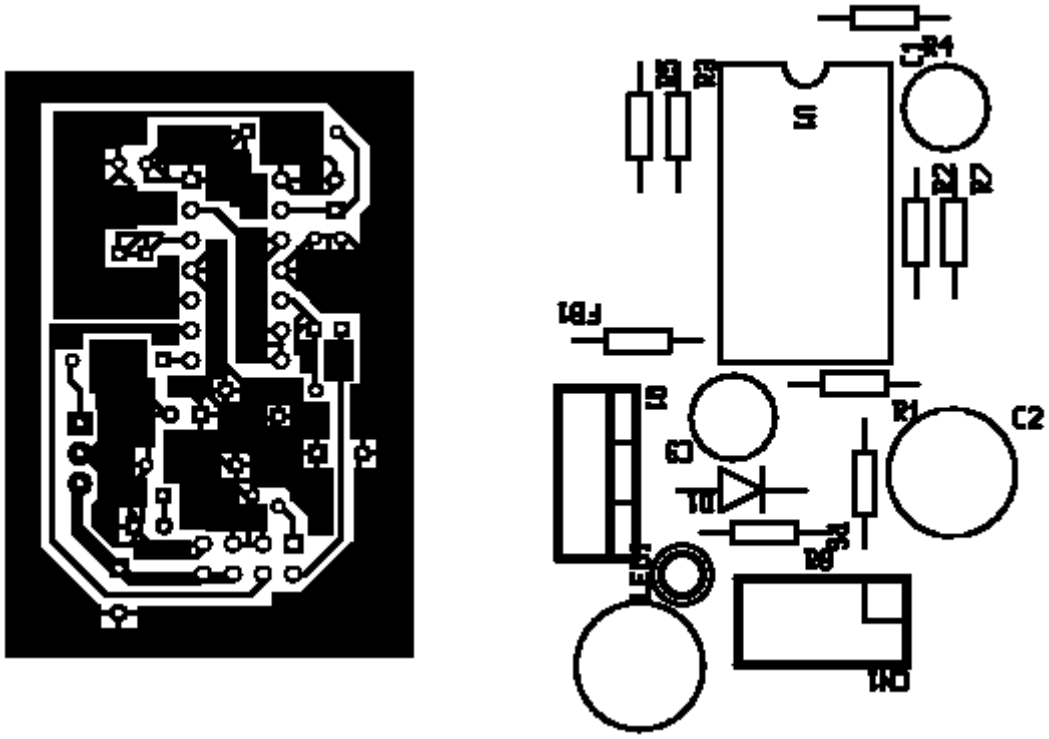
In the 24 Volt mode, regulator **U2** converts the 24 Volt supply to 12 Volts for running the **PWM** circuit, Q1 switches the 24 Volt load to ground just like it does for the 12 Volt load. See the schematic for instructions on wiring the circuit for 12 Volts or 24 Volts.

When running loads of 1 amp or less, no heat sink is needed on Q1, if you plan to switch more current, a heat sink with thermal grease is necessary. Q1 may be replaced with a higher current device such as an IRFZ34N. All of the current handling devices, switch S1, fuse F1, and the wiring between the FET, power supply, and load should be able to handle the maximum load current.

5.5.4 Construction

The prototype for this circuit was constructed on a regular IC proto board with parts and wires stuck into the proto board holes. One version of the finished circuit was used to make a variable speed DC fan, the fan was mounted on top of a small metal box and the **PWM** circuit was contained inside of the box.

A simple circuit board (see picture) was built using a **free circuit board CAD program**, PCB (1) that **runs on the Linux operating system**. The circuit board image was printed on a PostScript laser printer onto a mask transfer product called Techniks Press-n-Peel blue film (2). The printed on film is then ironed on to a cleaned piece of single sided copper clad board. The board is etched with **Ferric Chloride solution**. Holes are drilled with a fine gauge drill bit, parts are soldered in, and the board is wired to the power and load. This technique is great for producing working boards in a short time but is not suitable for large numbers of boards. A board pattern is shown in Fig 3, this may be photo-copied onto a piece of press-n-peel blue film. Alternately, the dead-bug construction method may be used, this involves taking a piece of blank copper PC board, gluing a wire-wrap IC socket to the board with 5 minute epoxy, then soldering all of the parts to the wire wrap pins. Grounded pins can be soldered directly to the copper board.



The unlabeled circular pattern is just a wire jumper.

Picture of PCB.

5.5.5 Alignment

No alignment is required with this circuit.

5.5.6 Use

This circuit will work as a DC lamp dimmer, small motor controller, and even as a small heater controller. It would make a great speed control for a solar powered electric train. The circuit has been tried with a 5 Amp electric motor using and IRFZ34N FET and worked ok, D1 may need to be replaced with a faster and higher current diode with some motors. The circuit should work in applications such as a bicycle motor drive system, if you experiment with this, be sure to include an easily accessible emergency power disconnect switch in case the FET shorts on.

Wire the circuit for 12 Volts or 24 Volts as per the schematic, connect the battery to the input terminals, and connect the load to the output terminals, be sure not to ground either output terminal or anything connected to the output terminals such as a motor case. Turn the potentiometer knob back and forth, the load should show variable speed or light.

5.5.7 Parts

U1:	LM324N quad op-amp
U2:	78L12 12 volt regulator
Q1:	IRF521 N channel MosFet
D1:	1N4004 silicon diode
LED1	Red LED
C1:	0.01uF ceramic disc capacitor, 25V
C2-C5:	0.1uF ceramic disk capacitor, 50V
R1-R4:	100K 1/4W resistor
R5:	47K 1/4W resistor
R6-R7:	3.3K 1/4W resistor
R8:	2.7K 1/4W resistor
VR1:	10K linear potentiometer
F1:	3 Amp, 28V DC fast blow fuse
S1:	toggle switch, 5 Amps

5.5.8 Parts Sources

Jameco 1-800-831-4242	**http://www.jameco.com/**
Digi-Key 1-800-DIGIKEY	**http://www.digikey.com/**

(1) PCB Software for Unix and Linux	(ftp://ftp.uni-ulm.de/pub/pcb/mirror/)
(2) Techniks, Inc P.O. Box 463 Ringoes, NJ 08551 908-788-8249 Press-N-Peel	(http://www.techniks.com/)
See the variations on this circuit for more ideas	(http://www.solorb.com/elect/solarcirc/pwm2/)
FC's Solar Circuits page.	http://www.solorb.com/elect/solarcirc/

5.6 PWM Motor/Light Controller

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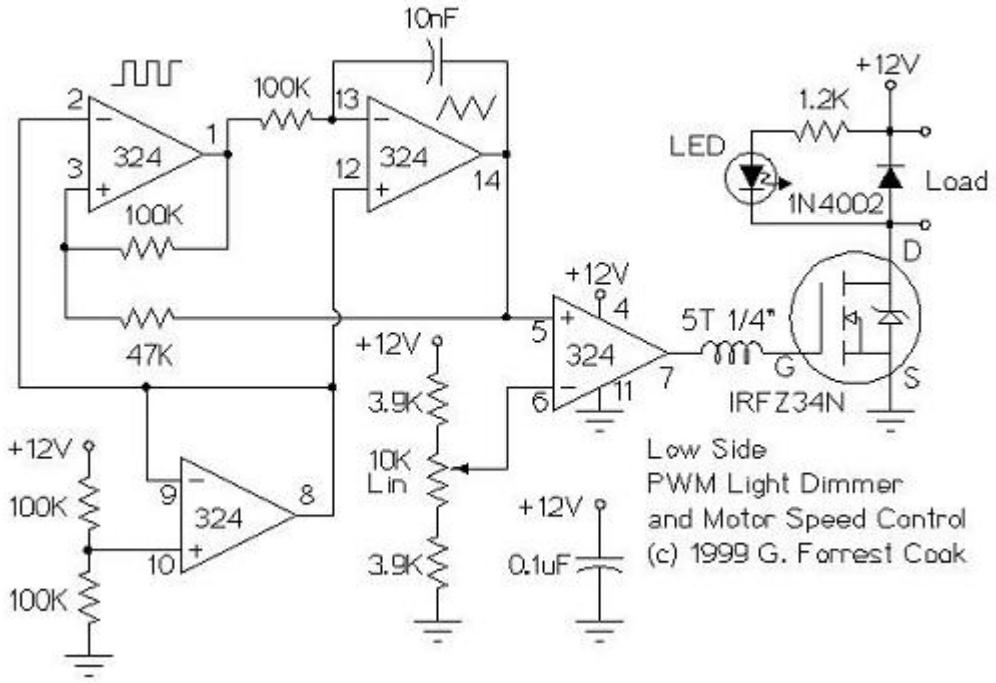
These two schematics are variations on **another** PWM circuit that I designed, (**http://www.solorb.com/elect/solarcirc/pwm1/**). The diagrams are for 12V operation only and there are high side (common ground) and low side (common +12V) versions. The low side version is in fact, identical to the original circuit when wired for 12V operation. The low side version allows the use of higher power and more inexpensive N Channel FETs, whereas the high side version, which uses P Channel FETs is used where common ground load wiring is a requirement. The inductor on the gate side of the power MOSFET transistor can be a ferrite bead or a few turns of wire wrapped around a 10 ohm, 1/4W resistor. The purpose of this inductor is to supress RF oscillation from the MOSFET.

This circuit can, in theory, switch a lot of current, an IRFZ34N MOSFET can handle over 35 Amps if connected to a proper heat sink. Inductive loads may require special care since they can generate large voltage spikes that can damage the MOSFET. Replacing the 1N4002 with a fast recovery diode may help absorb the reverse voltage kick when driving an inductive load such as a motor.

Note that the pwm control has an opposite effect on these two circuits, the low side version is on with a high pin 7 output voltage and the high side version is on with a low output.

In general, NMOS transistors like the IRFZ34N are lower cost and higher current compared to PMOS transistors like the IRF9540. Almost any power MOSFET transistor will work in these circuits, the load current should be lower than the transistor's maximum rating.

Note: if the circuit does not completely turn off and on when the 10K potentiometer is fully left and right, replace both of the 3.9K resistors with 3.3K resistors.



5.6.1 12V low side PWM Motor/Light Controller

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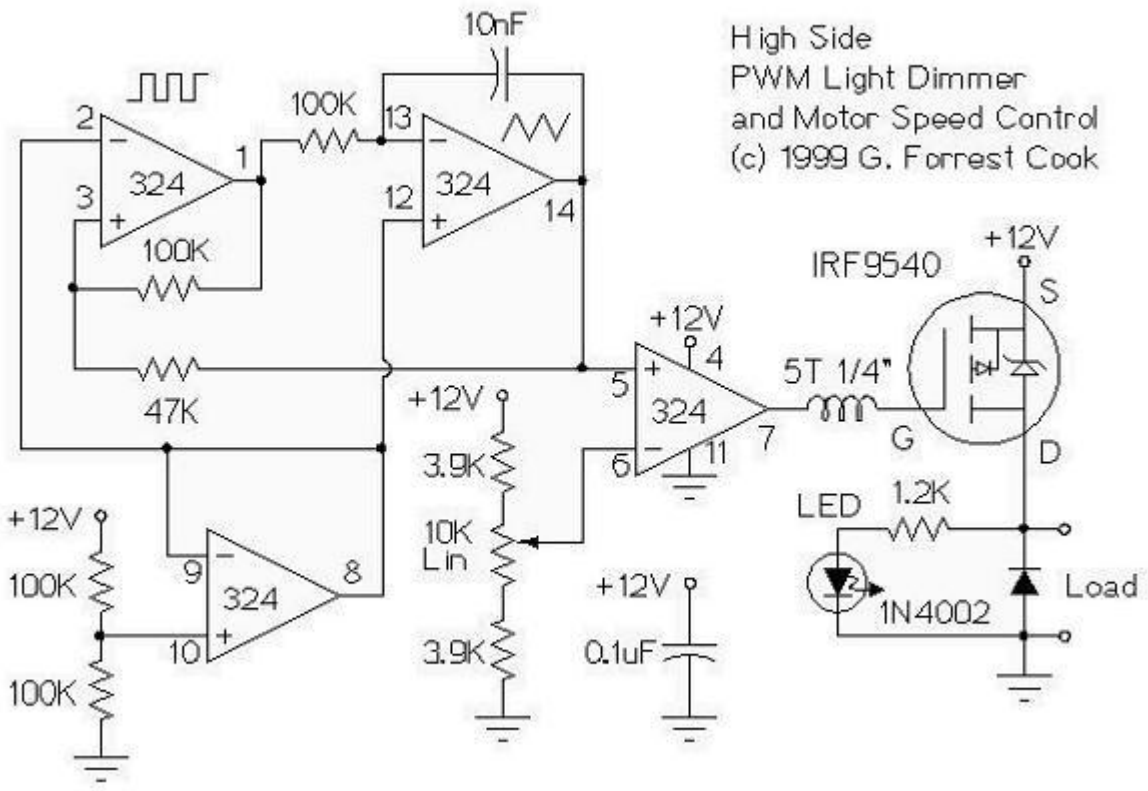
12V high side PWM Motor/Light Controller



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5.7 Proyectos.(4.2)