Project 2  
Digital Electronics  
Fall 2008  
Multipliers

The project consists of modeling two kinds of parallel multipliers using VHDL. The first multiplier to be considered is the Modified Booth Multiplier. The project report must contain the following sections:

1. Introduction: mentioning the importance of multiplication in digital signal processing.
2. Modified Booth Multiplier: briefly describing the Modified Booth Multiplier (Booth) and including a diagram of your design. The adder should be design for a 16-bit unsigned numbers. Additionally, discuss the modifications necessary to increase the wordlength from 16-bits to 32 and 64 bits.
3. VHDL Code: Including the design consideration of the Booth. The code must be properly documented by using comments. Additionally, the testbench must be included.
4. Simulation Results: The waveform obtained by simulating the code in ModelSim for Booth. Justify the testbench input signals used by explaining your reasoning behind the test pattern selected.
5. Select any of the following multiplier: Include a brief description of the selected multiplier
   a. Braun Multiplier
   b. Baugh-Wooley Multiplier
   c. Wallace Tree
6. VHDL Code: Including the design consideration of the selected multiplier. The code must be properly documented by using comments. Additionally, the testbench must be included
7. Simulation Results: The waveform obtained by simulating the code in ModelSim for the selected multiplier. Justify the testbench input signals used by explaining your reasoning behind the test pattern selected.
8. Comparison: Compare the Booth with the selected adder in terms of the gate count, the delay (find an analytical formula of the associated delay). Mention the drawbacks and advantages of the Booth and the selected adder.
9. Bibliography: Include all the references consulted for this project

Suggested References


